



Techniques for Formal Modelling and Verification on Dynamic Memory Allocators

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1. Importance and challenges
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2. Modular and stepwise refinement

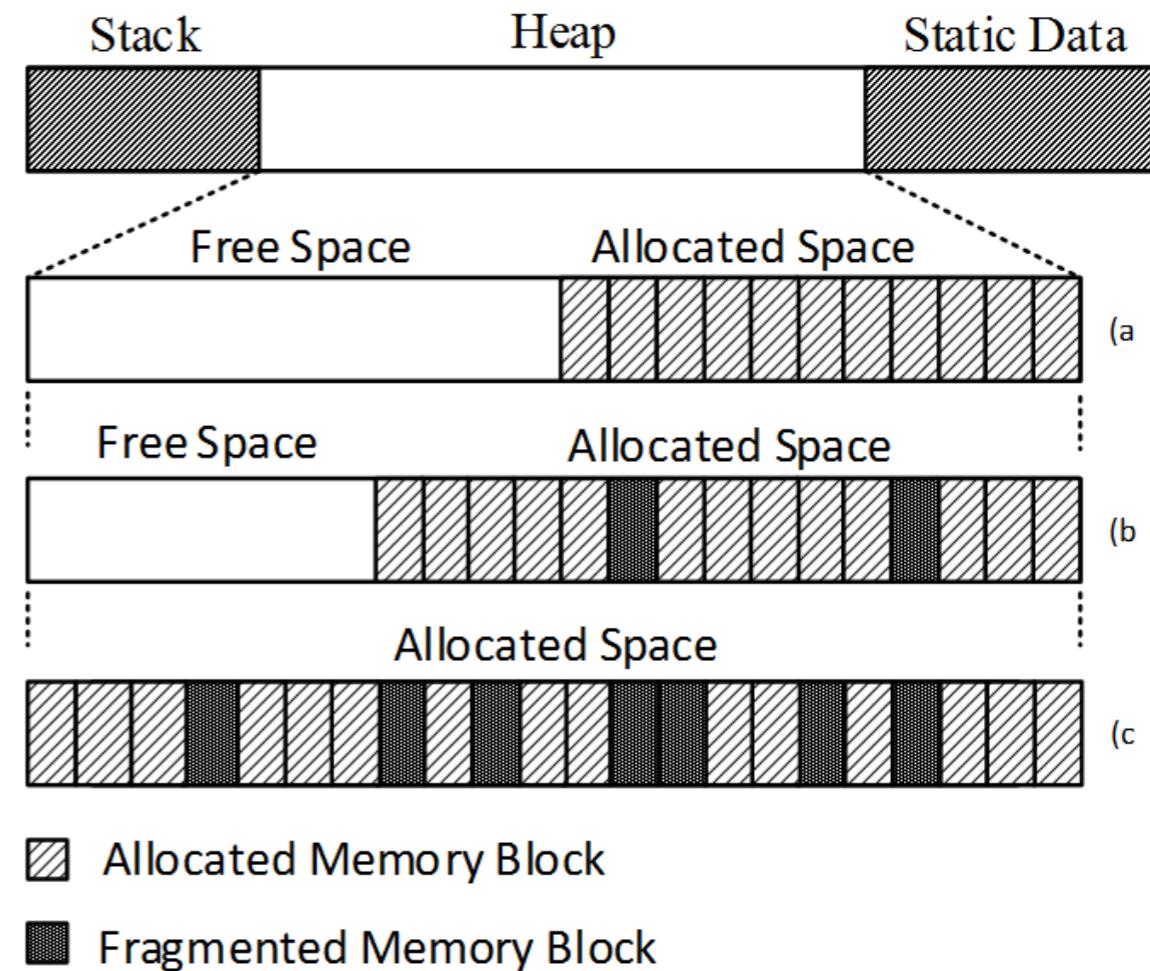
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1. Separation logic fragment **SLMA**
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Dynamic Memory Allocators

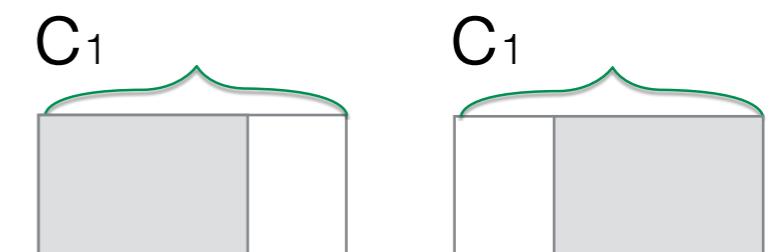
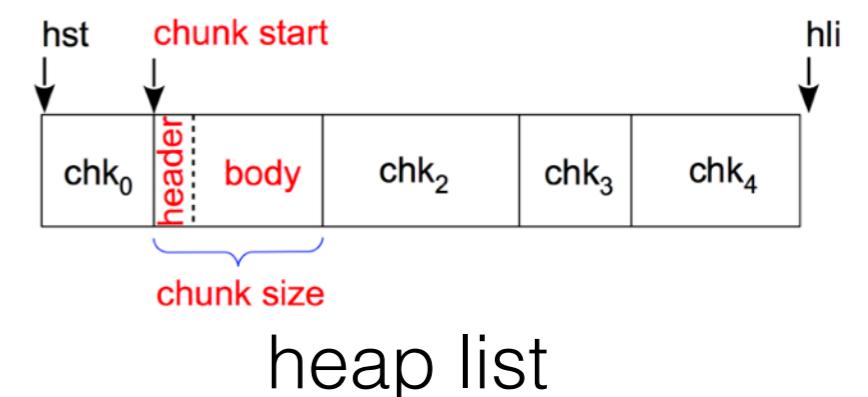
- Operating system, e.g., RTOS
- Programming language library
- Diverse features



```
void init(); //initialization
bool free(void* p); //deallocation
void* alloc(size_t sz); //allocation
void* realloc(void* p, size_t sz); //change size of p
```

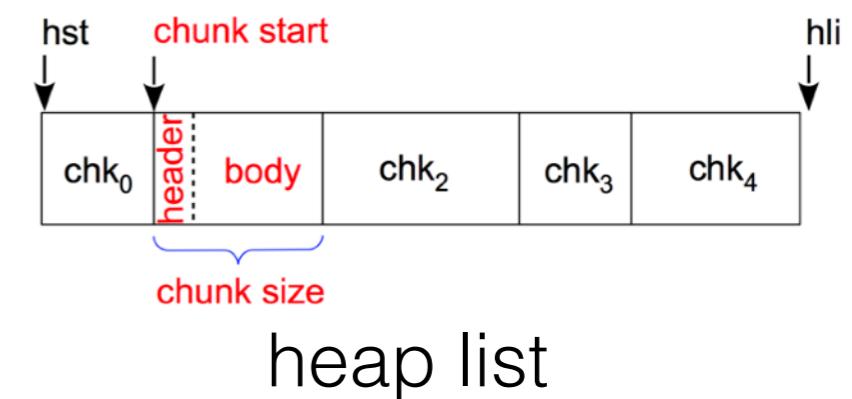
Design tactics

- heap list: singly / doubly linked list (SLL,DLL)
- fit policy: first fit, best fit, next fit
- splitting
- defragmentation strategy (coalescing policy)
- free chunks management (free list, eg., SLL, DLL)
- ...



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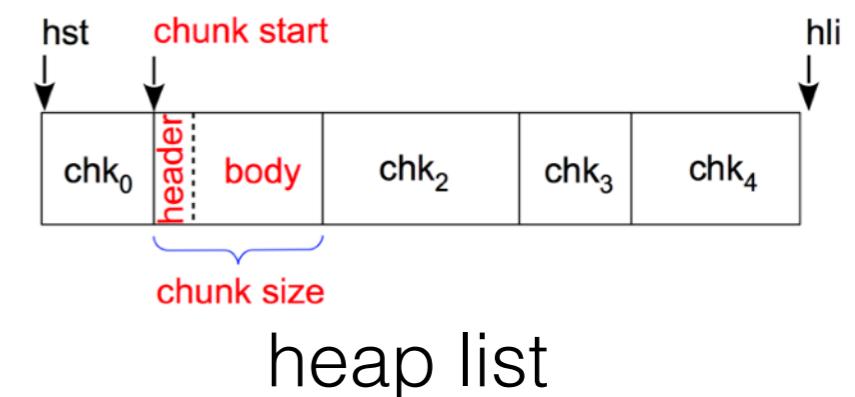


- *eager coalescing*
- *lazy coalescing*
- *no coalescing*

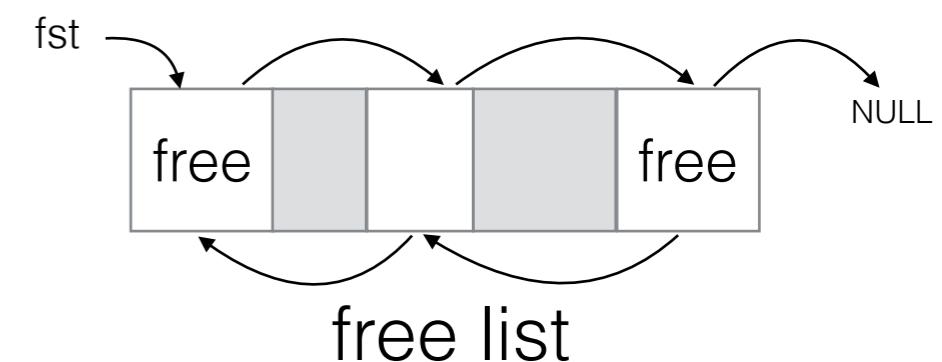
Dynamic Memory Allocators

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heap list

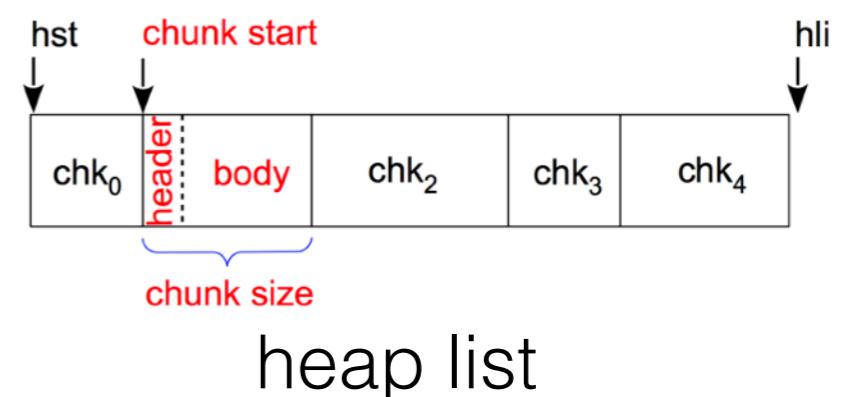


free list

Dynamic Memory Allocators

Properties

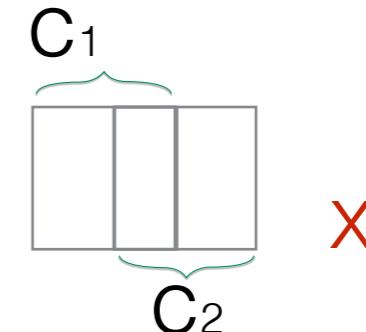
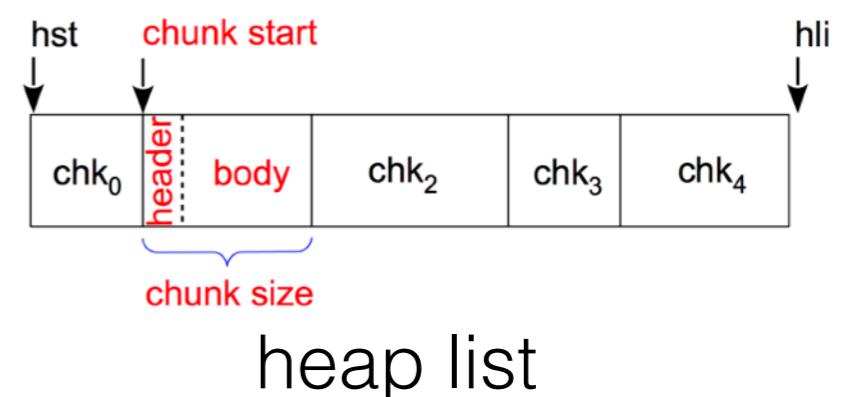
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- no overlapped chunks
- adjacent free chunks
- shape of heap/free list: cyclic, acyclic
- sorting of free list: address sorted/unsorted



Dynamic Memory Allocators

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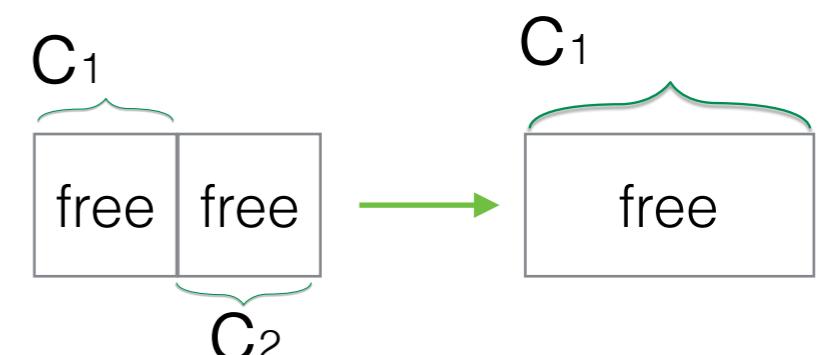
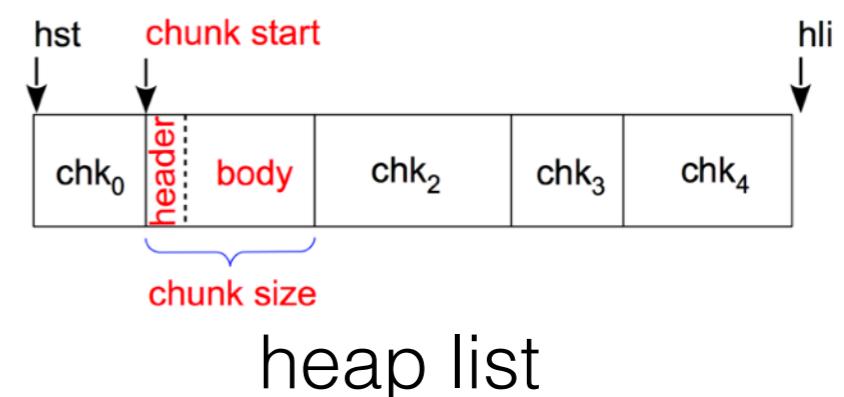
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Dynamic Memory Allocators

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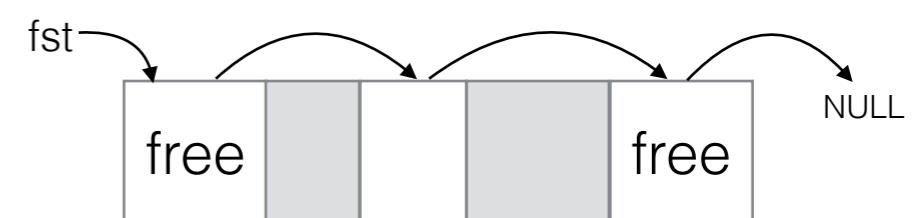
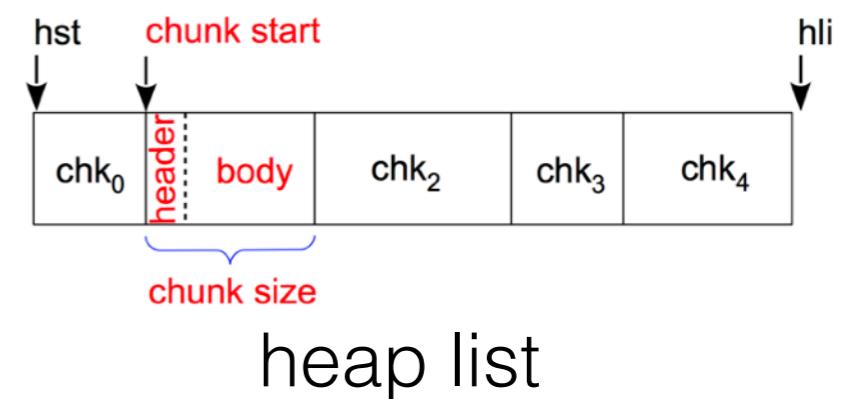
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Dynamic Memory Allocators

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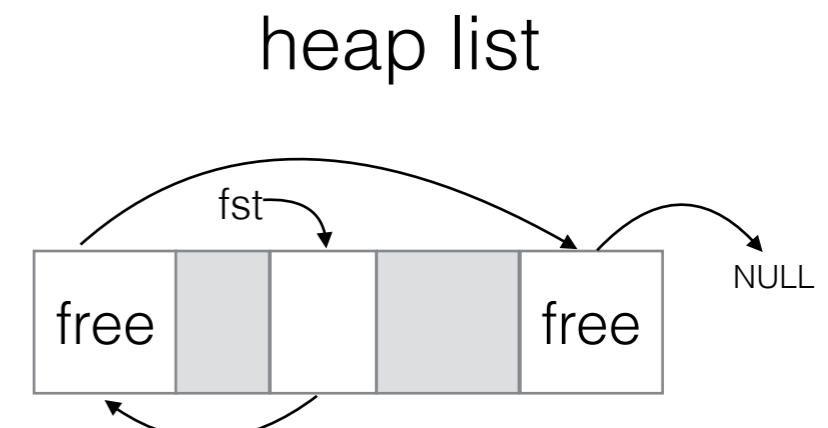
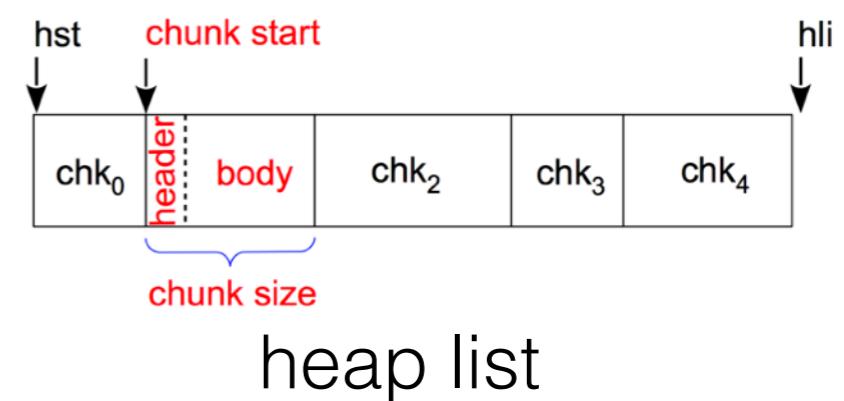
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Dynamic Memory Allocators

Properties

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- no overlapped chunks
- adjacent free chunks
- shape of free list: cyclic, acyclic
- sorting of free list: address sorted/unsorted



....

Each DMA has a set of tactics and properties

- 1.** How to find a way to formalize?
- 2.** How to design an abstract domain?

that apply to a large class of free-list DMAs, e.g.,

- IBM allocator: no heap-list, first-fit
- Kernighan&Ritchie alloc: eager coalescing, cyclic free-list, address sorted
- Lea's alloc: acyclic doubly linked free-list, unsorted, best-fit

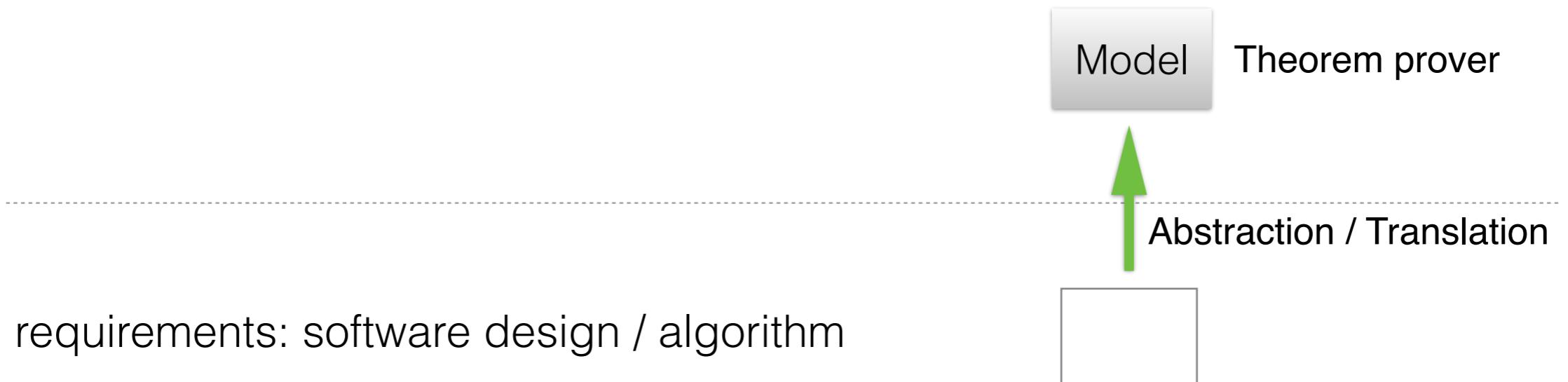
PART I:

Formal modelling based on refinement

Formalization of Dynamic Memory Allocators

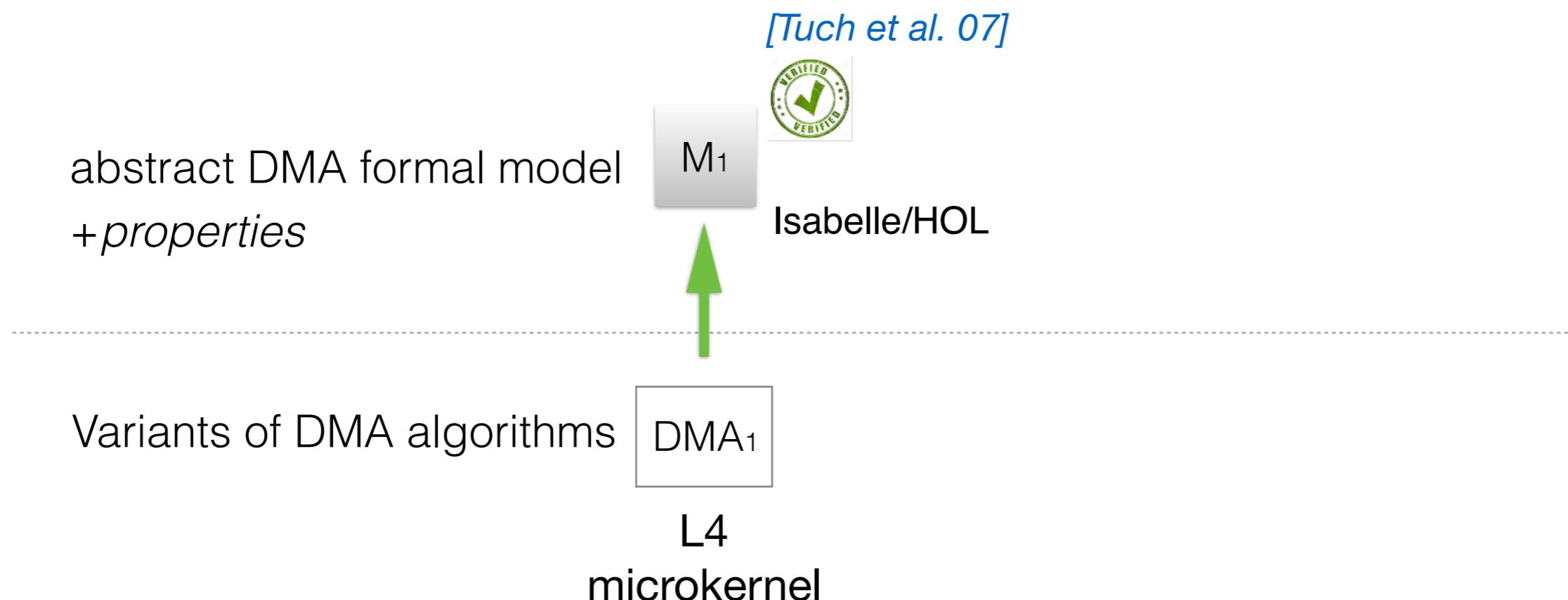
Procedure of Formalization

1. construct formal model (abstraction)
2. specify properties
3. auto-generate proof obligations
4. auto / interactive proof



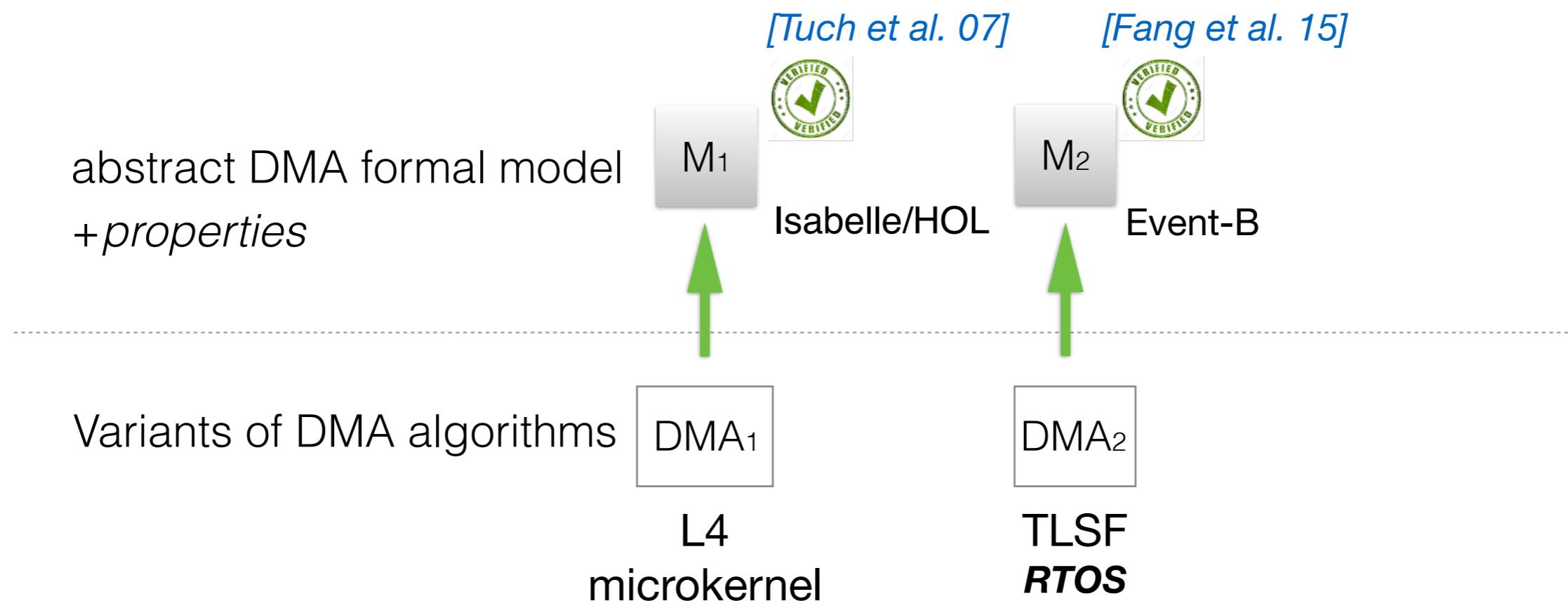
Formalization of Dynamic Memory Allocators

Different specification languages



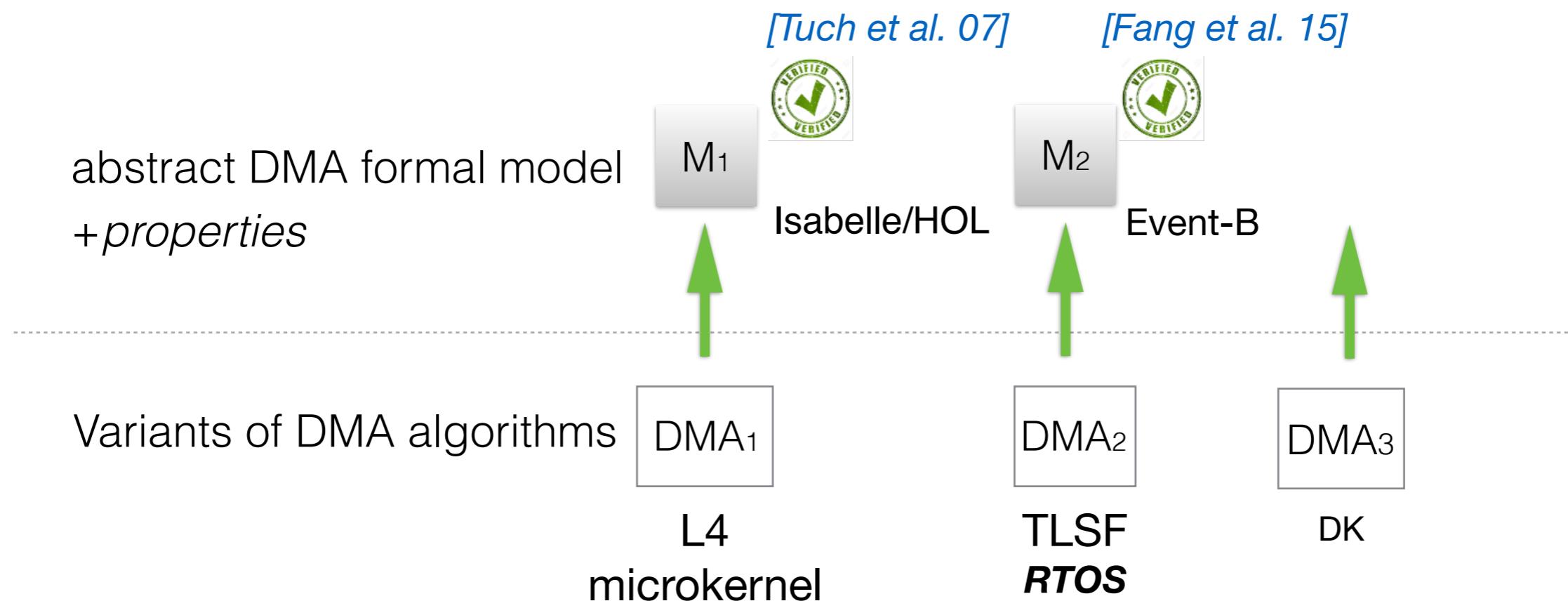
Formalization of Dynamic Memory Allocators

Different specification languages



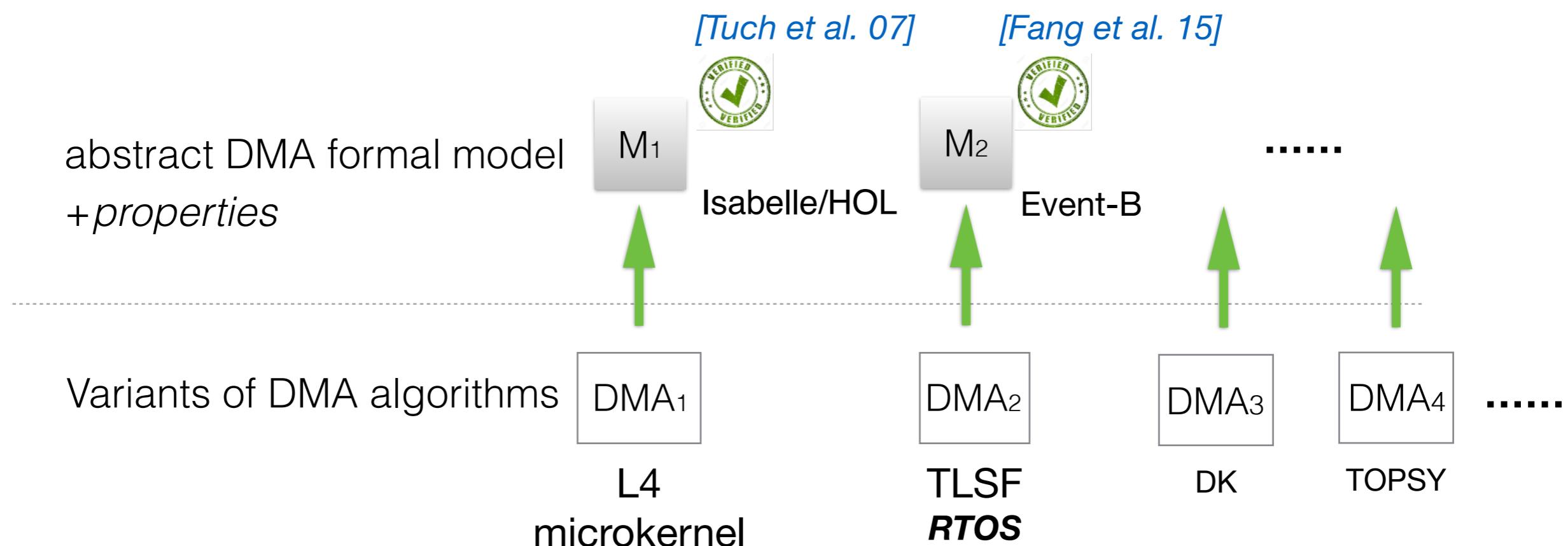
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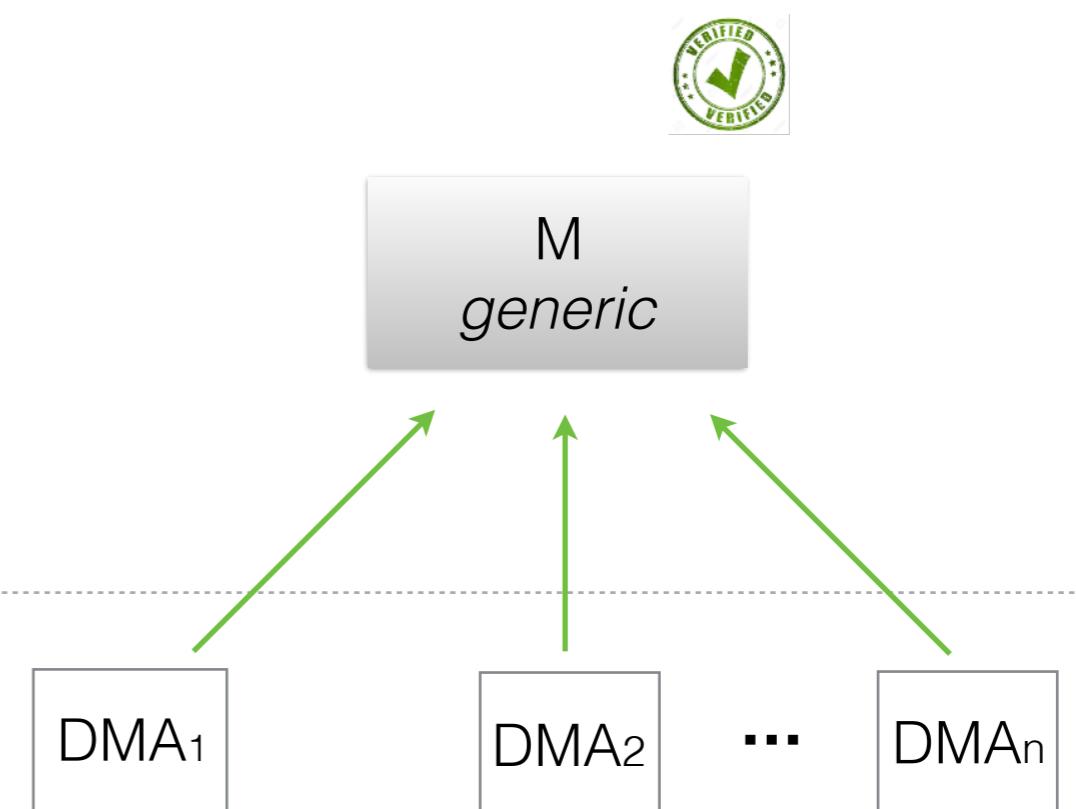


Formalization of Dynamic Memory Allocators

A generic framework of formalization

abstract DMA formal model
+*properties*

Variants of DMA algorithms

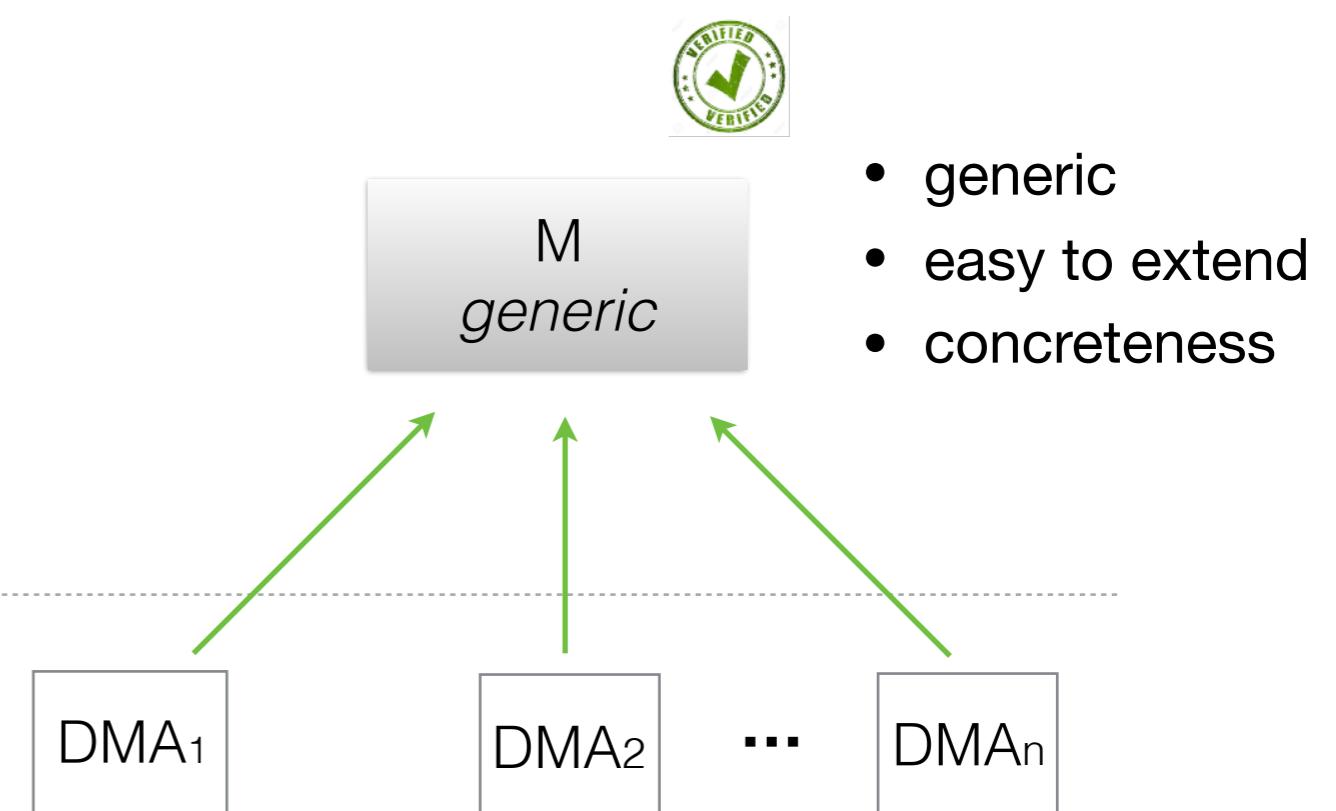


Formalization of Dynamic Memory Allocators

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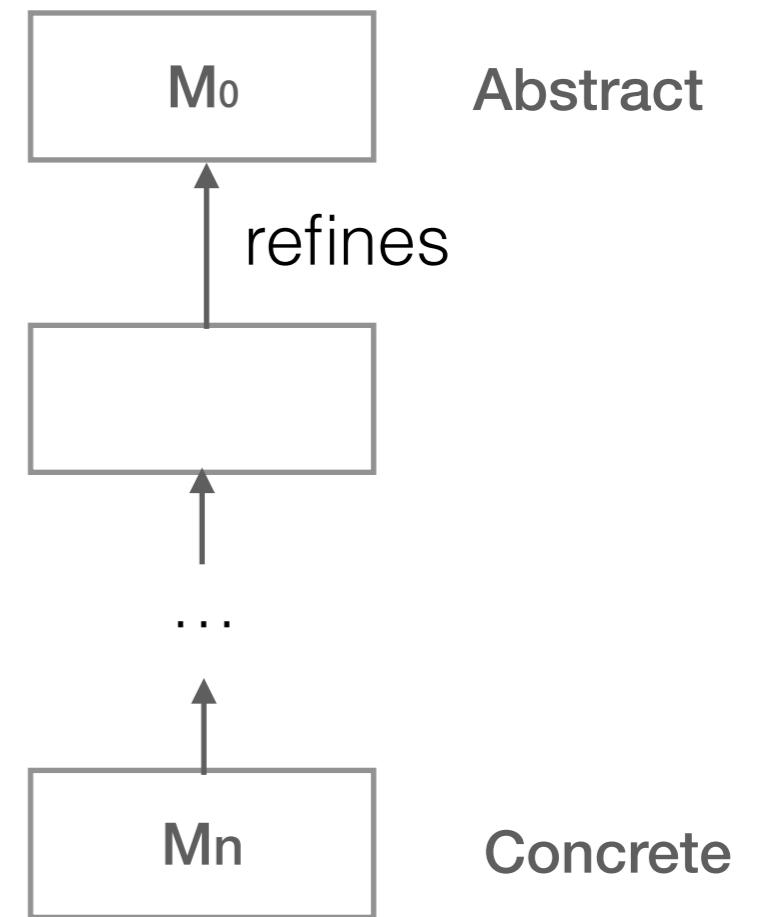
Variants of DMA algorithms



Formalization of Dynamic Memory Allocators

Strategy of formalization

1. Event-based state transition system
(Event-B modelling notation [\[Tuch et al. 07\]](#))
2. Stepwise refinement (top-down)

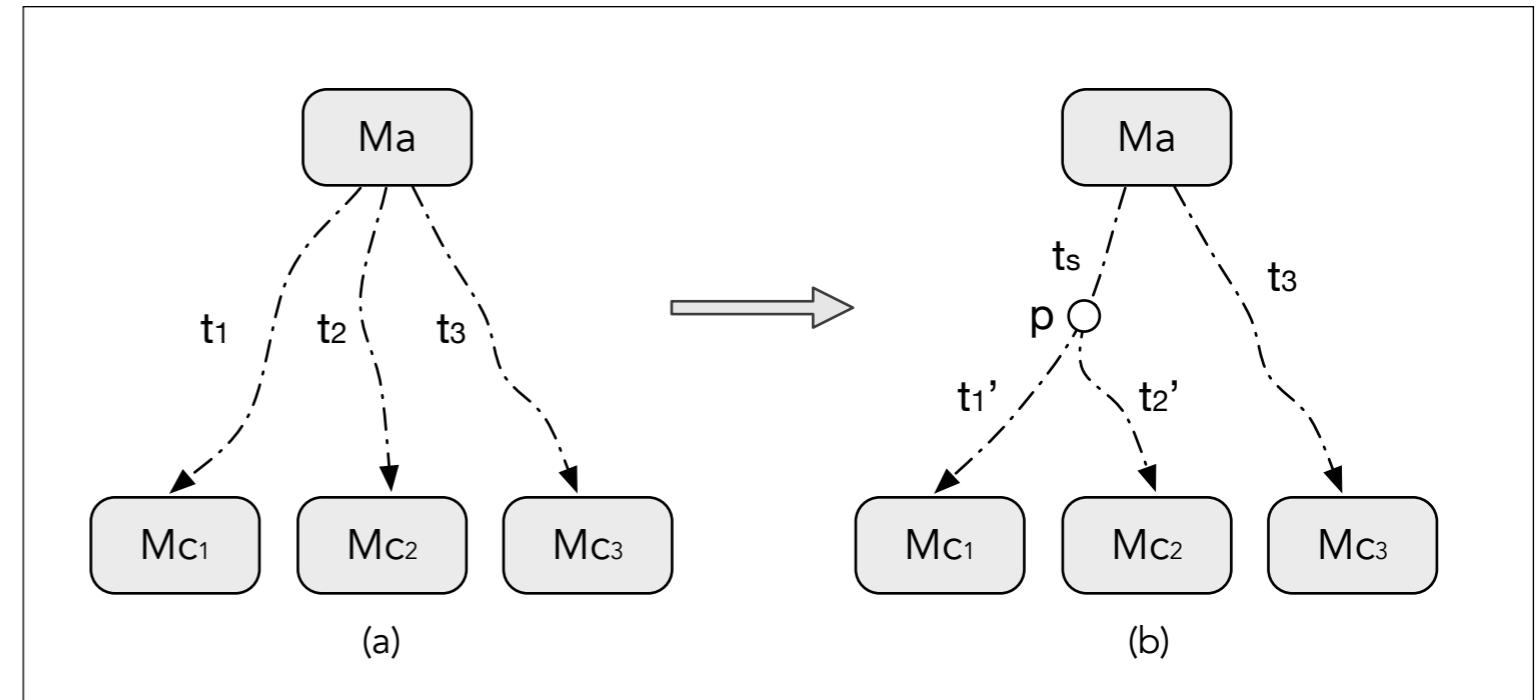


TLSF [\[Fang et al. 15\]](#)

Formalization of Dynamic Memory Allocators

Strategy of formalization

1. Event-base state transition system
(Event-B modelling notation [\[Tuch et al. 07\]](#))
2. Stepwise refinement (top-down)
3. Modular formalisation



Formalization of Dynamic Memory Allocators

Formalization steps

1. Most abstract model (common interface)

Case study	heap list			free list		fit
	linked	split	defrg.	shape	sort	
IBM [4]	addr, \rightarrow	—	—	—	—	F
DL-small [15]	size, \rightarrow	—	—	—	—	F
TOPSY [9]	size, \rightarrow	end	lazy	—	—	F
DKFF [14]	size, \rightarrow	start	early	A, \rightarrow	yes	F
DKBF [14]	size, \rightarrow	start	early	A, \rightarrow	yes	B
LA [3]	size, \rightarrow	start	early	A, \rightarrow	yes	F
DKNF [14]	size, \rightarrow	start	early	A, \rightarrow	yes	N
KR [12]	size, \rightarrow	start	early	C, \rightarrow	yes	N
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case studies

1

```
void init();
bool free(void* p);
void* alloc(size_t sz);
void* realloc(void* p, size_t sz);
```

interface for clients

Formalization of Dynamic Memory Allocators

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1 abstract model

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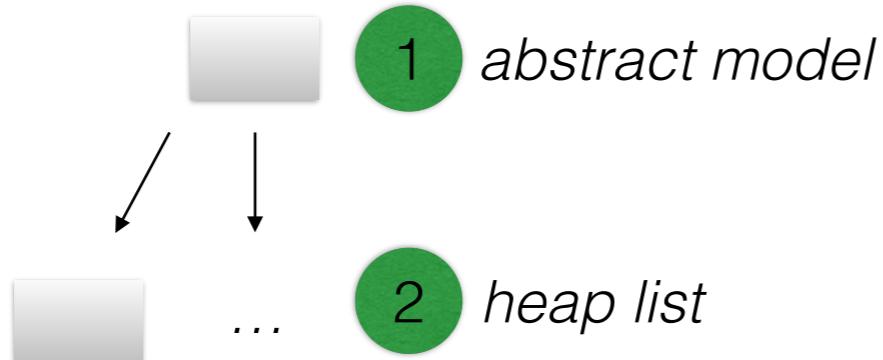
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interface for clients

Formalization of Dynamic Memory Allocators

Formalization steps

1. Most abstract model (common interface)
2. heap list types



2

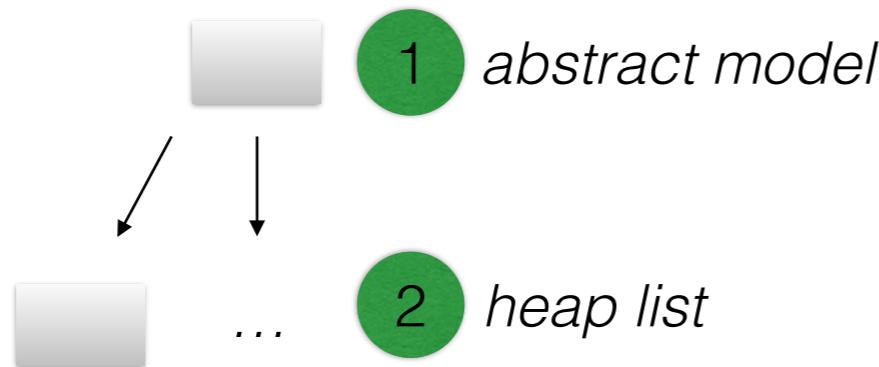
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case studies

Refined allocation

Abstract allocation

Alloc
- status updating

1



Alloc

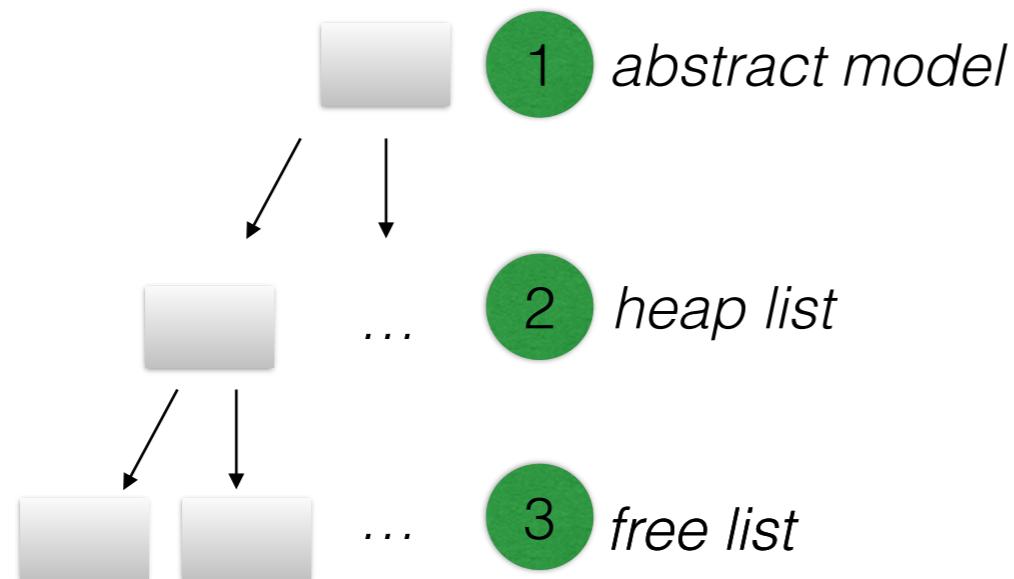
- searching
- splitting
- ...

2

Formalization of Dynamic Memory Allocators

Formalization steps

1. Most abstract model (common interface)
2. heap list types
3. Free list types



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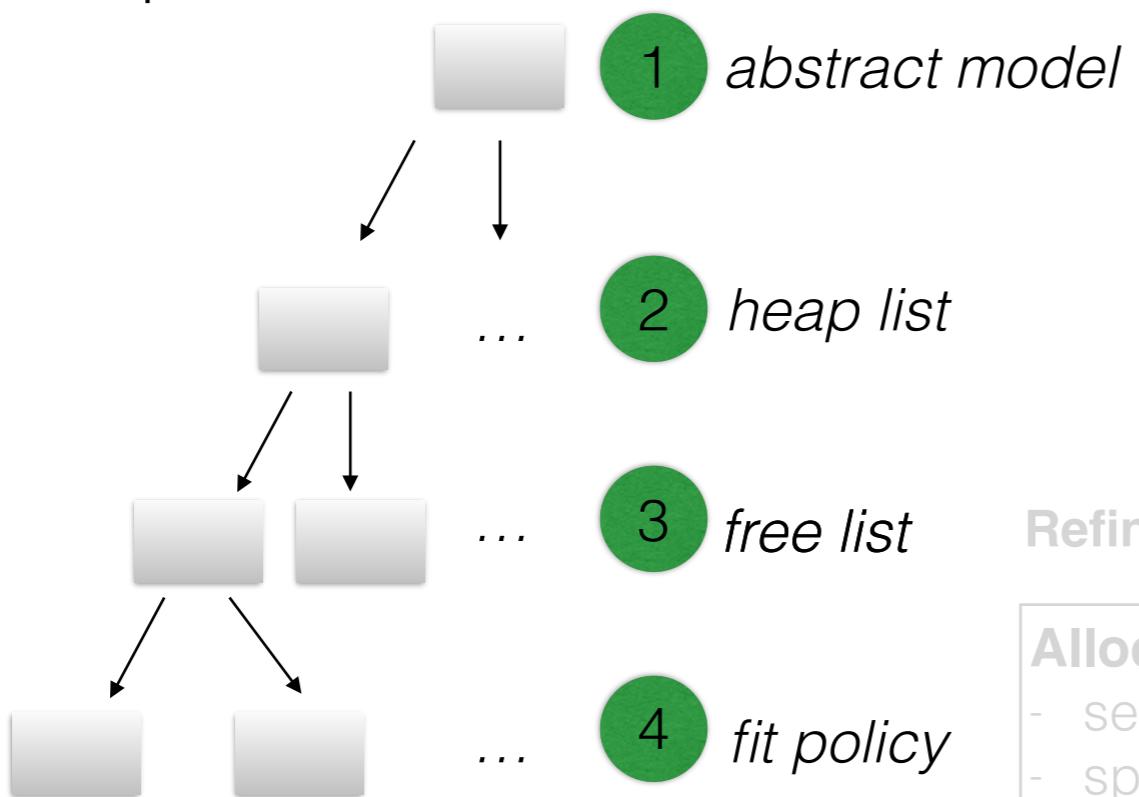
case studies

3

Formalization of Dynamic Memory Allocators

Formalization steps

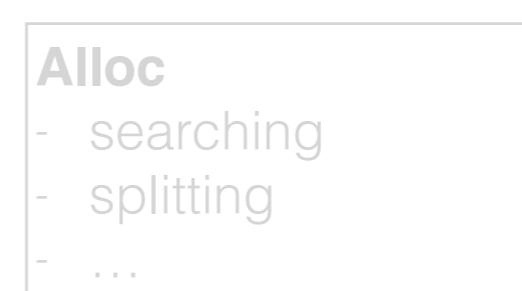
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3. Free list types
4. Fit policies



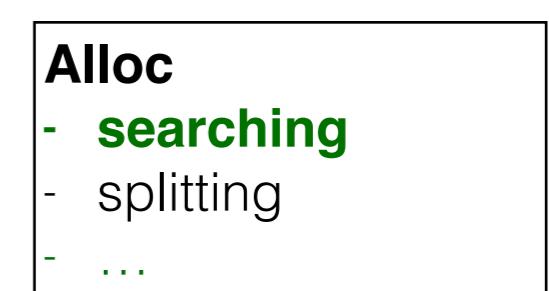
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case studies

Refined allocation



Refined allocation



3

4

Formalization of Dynamic Memory Allocators

Hierarchy of models

1. Extensible hierarchy
2. Clear refinement principles
3. Covers diverse DMAs

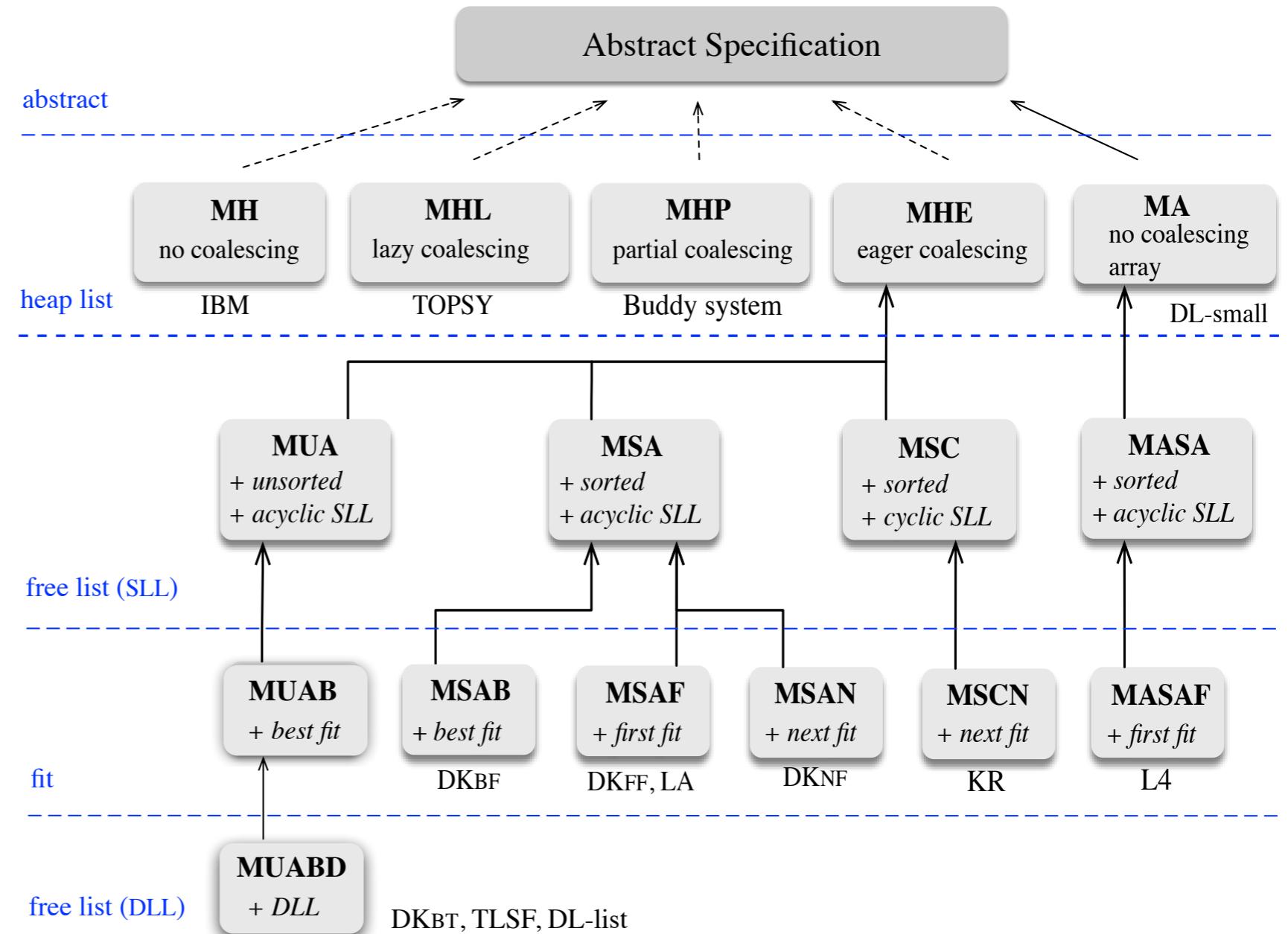


fig. A partial view of the hierarchy of models and the case studies it covers

Formalization of Dynamic Memory Allocators

Hierarchy of models

Theorem: Models consistency

Each model is proved.

Theorem: Refinement correctness

*The refinement relations between
models are valid.*

Models	LOC	Proof obligations	Automatically discharged	Interactive proofs
MH	114	39	27(69%)	12(31%)
MHL	176	8	8(100%)	0(0%)
MHE	183	82	58(70%)	24(30%)
MHP	383	143	140(98%)	3(2%)
MA	168	20	20(100 %)	0 (0%)

Models	LOC	Proof obligations	Automatically discharged	Interactive proofs
MUA	219	36	30(83%)	6(17%)
MSA	197	41	27(66%)	14(34%)
MSC	205	37	30(82%)	7(18%)
MSAB	202	2	2(100%)	0(0%)
MSAF	202	2	2(100%)	0(0%)
MSAN	200	2	2(100%)	0(0%)
MSCN	221	40	36(88%)	4(12%)
MUABD	241	9	9(100%)	0(0%)
MASA	182	21	18(85.6%)	3(14.4%)
MASF	186	2	2(100%)	0(0%)

fig. Statistics on proofs

ISMM'17, SCIS'17 (journal)

PART II:

Algorithmic verification by static analysis

Dynamic Memory Allocators implementation

- Small but critical piece of code
- Variety of policies and techniques [Wilson et al 95]
- Combines low-level (**pointer arithmetics**, system calls) and high level (**dynamic data structures**) code
- Complex properties (invariants) on both levels

Properties

- Spatial properties for structure of disjoint memory
- Intricate numerical properties for data, e.g., memory's size and content
- Different levels of abstractions (heap and free lists)

Aim: automatically infer DMA properties

- Logical abstract domain on Separation Logic [O'Hearn, Reynolds, Yang'01]
- Combination of domains
- Hierarchical abstraction

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Static analysis based on abstract interpretation [Cousot 77,79]

- Design **abstract domains** to capture properties
- Lattice operators (S , \sqsubseteq , \sqcup , \sqcap , \perp , \top)
- Termination or acceleration of iteration (widening operation)
- Abstract transformers (assignments, condition tests, ...)

Logic-based shape analysis

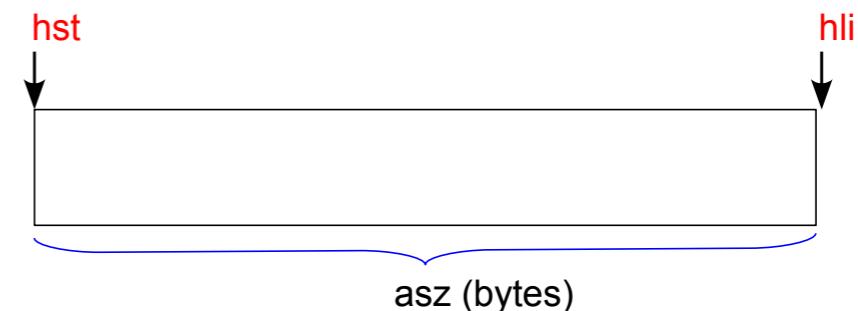
- Abstract elements uses formulae from logic [Distefano et al 06]
- Entailment represents partial order ($\phi \Rightarrow \psi \Leftrightarrow \phi \sqsubseteq \psi$)

Memory Abstraction with Inductive Segments

Separation logic with inductive predicates

- Atomic predicates (raw memory region)
- Inductively-defined predicates (disjoint memory blocks)
- Separating conjunction $\phi \star \psi$

Raw memory region



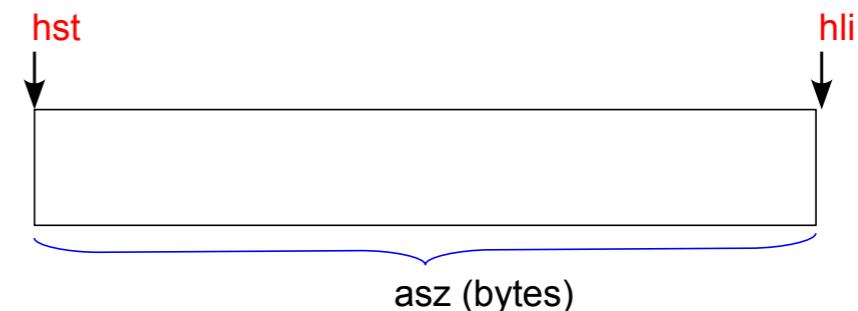
```
void minit(int asz)
{ ... hst=sbrk(asz); hli=sbrk(0); ... }
```

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Raw memory region



```
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{ ... hst=sbrk(asz); hli=sbrk(0); ... }
```

$$\text{blk}(hst; hli) \wedge hli - hst = asz$$

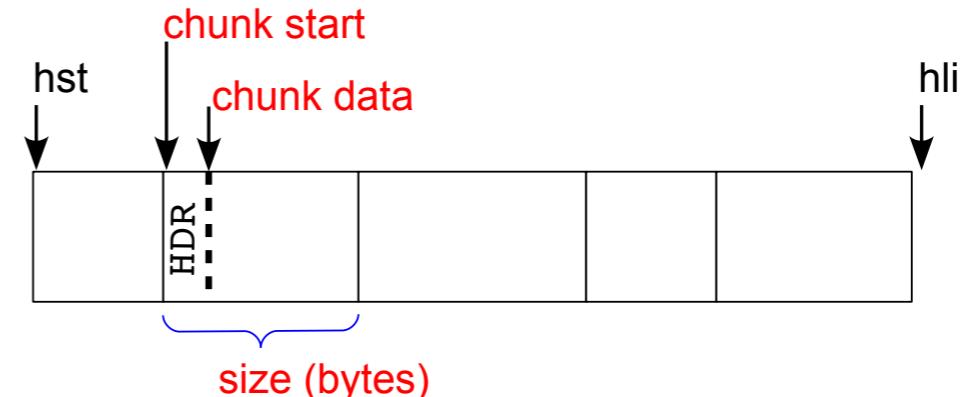
[Calcagno et al' 06]

Memory Abstraction with Inductive Segments

Separation logic with inductive predicates

- Atomic predicates (raw memory region)
- Inductively-defined predicates (disjoint memory blocks)
- Separating conjunction $\phi \star \psi$

Chunk region



```
typedef struct hdr_s {
    size_t size;
    bool isfree;
    struct hdr_s *fnx; } HDR;
```

$\text{chk}(hst; a_1) \star \text{chk}(a_1; a_2) \star \dots \star \text{chk}(a_n; hli)$

$\text{chk}(X; Y) \triangleq \exists Z. \text{chd}(X; Z) \star \text{blk}(Z; Y) \wedge Y - X = X.\text{size}$

[O'Hearn et al'01, Calcagno et al'06]

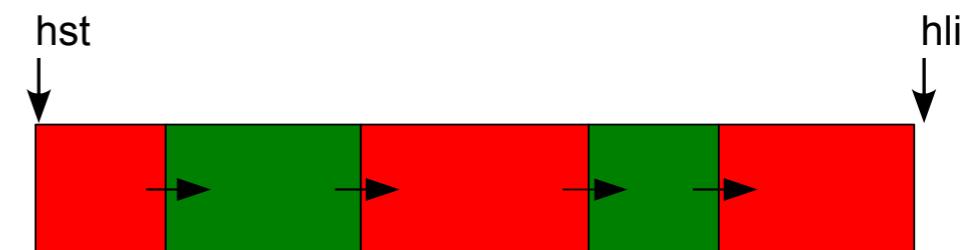
$\text{chd}(X; Y) \triangleq \text{blk}(X; Y) \wedge Y - X = |\text{HDR}| \wedge X \equiv_{|\text{HDR}|} 0$

Memory Abstraction with Inductive Segments

Separation logic with inductive predicates

- Atomic predicates (raw memory region)
- Inductively-defined predicates (disjoint memory blocks)
- Separating conjunction $\phi \star \psi$

Heap list

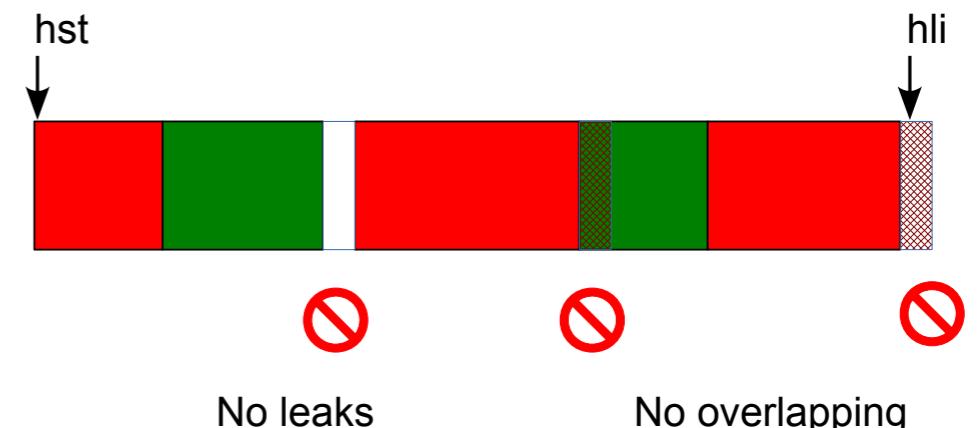


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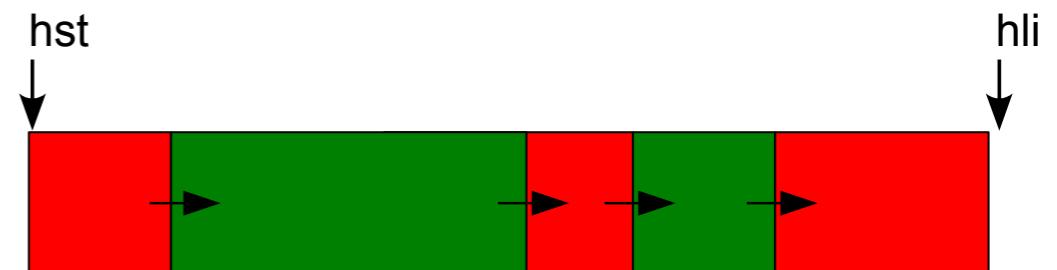
$$\begin{aligned} \text{hls}(X; Y)[W] &\triangleq \text{emp} \wedge X = Y \wedge W = \epsilon \\ &\vee \exists Z, W' \cdot \text{chk}(X; Z) \star \text{hls}(Z; Y)[W'] \wedge W = [X]. W' \end{aligned}$$

Memory Abstraction with Inductive Segments

Separation logic with inductive predicates

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Heap list with coalescing policy



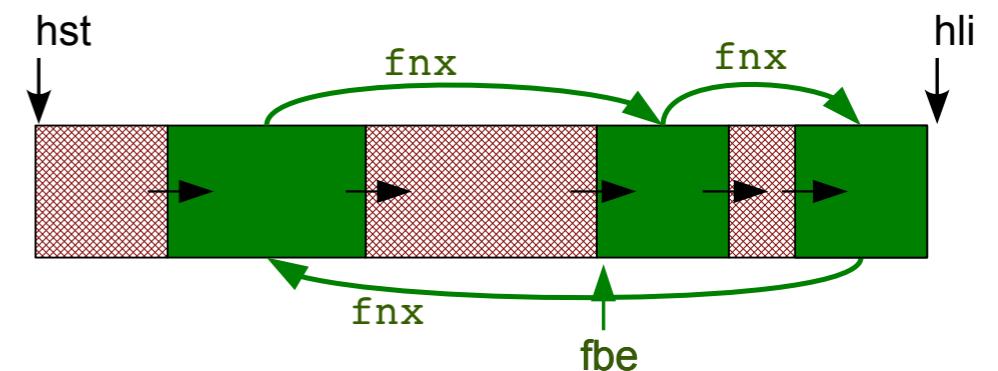
$$\begin{aligned} \text{hlsc}(X, f_x; Y, f_y)[W] &\triangleq \text{emp} \wedge X = Y \wedge W = \epsilon \wedge 0 \leq f_x + f_y \leq 1 \\ &\vee (\exists Z, W', f \cdot \text{chk}(X; Z) \star \text{hlsc}(Z, f; Y, f_y)[W'] \wedge W = [X] . W' \\ &\quad \wedge f = X \cdot \text{isfree} \wedge 0 \leq X \cdot \text{isfree} + f_y \leq 1) \end{aligned}$$

Memory Abstraction with Inductive Segments

Separation logic with inductive predicates

- Atomic predicates (raw memory region)
- Inductively-defined predicates (disjoint memory blocks)
- Separating conjunction $\phi \star \psi$

Free list

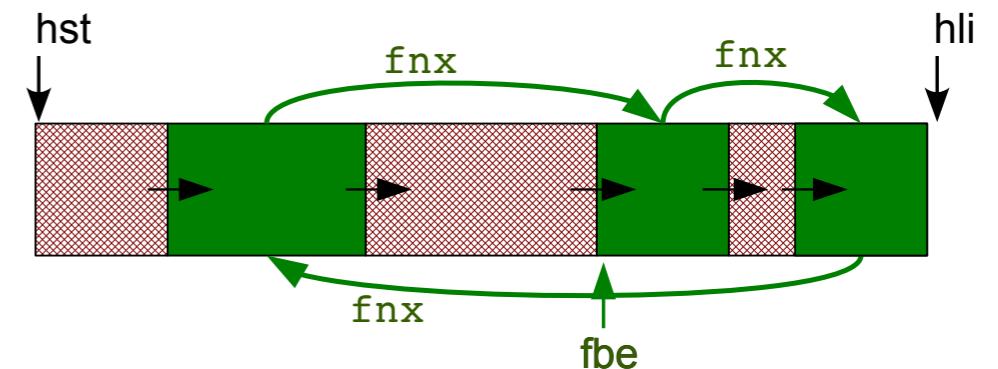


Memory Abstraction with Inductive Segments

Separation logic with inductive predicates

- Atomic predicates (raw memory region)
- Inductively-defined predicates (disjoint memory blocks)
- Separating conjunction $\phi \star \psi$

Free list



$$\text{fls}(X; Y)[W] \triangleq \text{emp} \wedge X = Y \wedge W = \epsilon$$

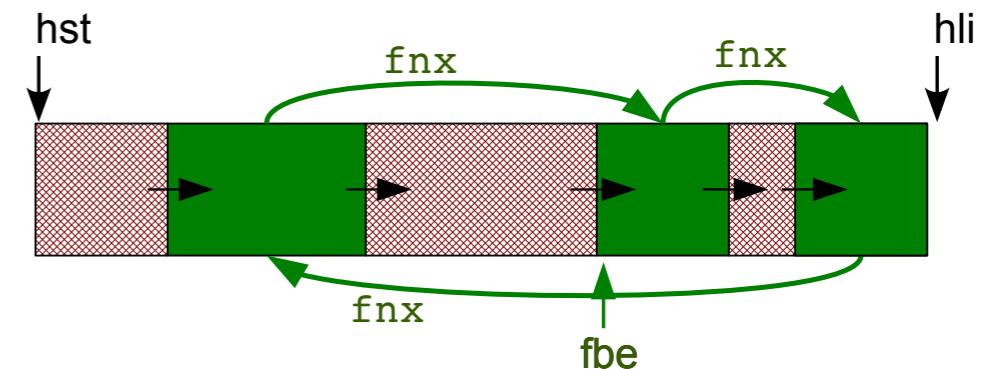
$$\vee \exists Z, W' \cdot \text{fck}(X; Z) \star \text{fls}(Z; Y)[W'] \wedge W = [X].W' \wedge X \neq Y$$

Memory Abstraction with Inductive Segments

Separation logic with inductive predicates

- Atomic predicates (raw memory region)
- Inductively-defined predicates (disjoint memory blocks)
- Separating conjunction $\phi \star \psi$

Free list



$$\text{fls}(X; Y)[W] \triangleq \text{emp} \wedge X = Y \wedge W = \epsilon$$

$$\vee \exists Z, W' \cdot \text{fck}(X; Z) \star \text{fls}(Z; Y)[W'] \wedge W = [X]. W' \wedge X \neq Y$$

$$\text{hls}(hst; hli)[W_H] \boxed{\exists} \exists Z, W' \cdot \text{fck}(fbe; Z) \star \text{fls}(Z; fbe)[W'] \wedge W_F = [fbe]. W'$$

combination symbol

Separation Logic fragment: SLMA

Spatial part of SLMA

$$\begin{aligned}\Sigma_H ::= & \text{ emp } | X \mapsto x | \text{blk}(X; Y) | \text{chd}(X; Y) | \text{chk}(X; Y) | \Sigma_H \star \Sigma_H | \\ & \text{hls}(X; Y)[W] | \text{hlsc}(X, i; Y, j)[W] \\ \Sigma_F ::= & \text{ emp } | \text{fck}(X; Y) | \text{fls}(X; Y)[W] | \text{flso}(X, i; Y, j) | \Sigma_F \star \Sigma_F\end{aligned}$$

Hierarchical conjunction of spatial formulas

$$\Sigma ::= \Sigma_H \ni \Sigma_F$$

Separation Logic fragment: SLMA

Spatial part of SLMA

$$\begin{aligned}\Sigma_H ::= & \text{emp} \mid X \mapsto x \mid \text{blk}(X; Y) \mid \text{chd}(X; Y) \mid \text{chk}(X; Y) \mid \Sigma_H \star \Sigma_H \mid \\ & \text{hls}(X; Y)[W] \mid \text{hlsc}(X, i; Y, j)[W] \\ \Sigma_F ::= & \text{emp} \mid \text{fck}(X; Y) \mid \text{fls}(X; Y)[W] \mid \text{flso}(X, i; Y, j) \mid \Sigma_F \star \Sigma_F\end{aligned}$$

Hierarchical conjunction of spatial formulas

$$\Sigma ::= \Sigma_H \ni \Sigma_F$$

By semantics:

Σ_H : sequence of addresses in the heap list

Σ_F : sequence of addresses in the free list

To specify overlapping of memory region, then \ni requires

$$\forall X \in W_F \Rightarrow X \in W_H$$

Separation Logic fragment: SLMA

Spatial part of SLMA

$$\begin{aligned}\Sigma_H ::= & \text{emp} \mid X \mapsto x \mid \text{blk}(X; Y) \mid \text{chd}(X; Y) \mid \text{chk}(X; Y) \mid \Sigma_H \star \Sigma_H \mid \\ & \text{hls}(X; Y)[W] \mid \text{hlsc}(X, i; Y, j)[W] \\ \Sigma_F ::= & \text{emp} \mid \text{fck}(X; Y) \mid \text{fls}(X; Y)[W] \mid \text{flso}(X, i; Y, j) \mid \Sigma_F \star \Sigma_F\end{aligned}$$

Hierarchical conjunction of spatial formulas

$$\Sigma ::= \Sigma_H \ni \Sigma_F$$

Pure formulas as location (sequence) and numerical constrains

$$\begin{array}{ll}\Pi ::= A \mid \Pi_{\forall} \mid \Pi_W & \Pi_{\forall} ::= \forall X \in W \cdot A_G \Rightarrow A_U \mid \Pi_{\forall} \wedge \Pi_{\forall} \\ L ::= X \mid X.\text{fnx} & \Pi_W ::= W_H = w \wedge W_F = w \\ A ::= L - L\#t \mid \Delta \mid A \wedge A & w ::= \epsilon \mid [x] \mid W \mid w.w\end{array}$$

Expressiveness of SLMA

SLMA captures the complex invariants of DMA

First-fit: (choice of a free chunk of req size)

$$\begin{aligned} \text{hls}(hst; \text{hli})[W_H] \supseteq & \text{ fls(fbe; } Y_2)[W_1] \star \text{fck}(Y_2; Y_3) \star \text{fls}(Y_3; \text{nil})[W_2] \\ \wedge & Y_2 \cdot \text{size} \geq req \wedge \forall X \in W_1 \cdot X \cdot \text{size} < req \\ \wedge & W_F = W_1 \cdot [Y_2] \cdot W_2 \end{aligned}$$

Best-fit:

$$\begin{aligned} \text{hls}(hst; \text{hli})[W_H] \supseteq & \text{ fls(fbe; } Y_2)[W_1] \star \text{fck}(Y_2; Y_3) \star \text{fls}(Y_3; \text{nil})[W_2] \\ \wedge & Y_2 \cdot \text{size} \geq req \wedge \forall X \in W_1, W_2 \cdot X \cdot \text{size} \geq req \Rightarrow X \cdot \text{size} > Y_2 \cdot \text{size} \\ \wedge & W_F = W_1 \cdot [Y_2] \cdot W_2 \end{aligned}$$

Decidability of SLMA

Satisfiability problem for SLMA is undecidable

- Decidable pure part of SLMA for integer constraints Π_N
- Undecidable array logic fragment Π_W

Entailment checking fro SLMA is undecidable

- Undecidable entire pure part of SLMA (sequence constrains)
- Undecidable spatial part (fragment of SL with inductive predicates and data constraints)

Abstract domain

1. Numerical domain *[Apron]* (polyhedra) - **arithmetic constraints** $\Pi_N \in \mathbb{N}^\#$

$$\mathcal{N}^\# = (\mathbb{N}^\#, \sqsubseteq^{\mathbb{N}}, \sqcup^{\mathbb{N}}, \sqcap^{\mathbb{N}}, \perp^{\mathbb{N}}, \top^{\mathbb{N}}), \quad \nabla^{\mathbb{N}}$$

Logic-based abstract domain

Abstract domain

1. Numerical domain *[Apron]* (polyhedra) - **arithmetic constraints** $\Pi_N \in \mathbb{N}^\#$

$$\mathcal{N}^\# = (\mathbb{N}^\#, \sqsubseteq^{\mathbb{N}}, \sqcup^{\mathbb{N}}, \sqcap^{\mathbb{N}}, \perp^{\mathbb{N}}, \top^{\mathbb{N}}), \quad \nabla^{\mathbb{N}}$$

2. Data words domain *[Bouajjani et al'11]* - **sequence constraints** $\Pi_W \in \mathbb{W}^\#$

$$\mathcal{D}^\# = (\mathbb{W}^\#, \sqsubseteq^{\mathbb{W}}, \sqcup^{\mathbb{W}}, \sqcap^{\mathbb{W}}, \perp^{\mathbb{W}}, \top^{\mathbb{W}}), \quad \nabla^{\mathbb{W}}$$

Logic-based abstract domain

Abstract domain

3. Shape abstract domain - **spatial part** Σ

$$\mathcal{G}^\sharp = (\mathbb{G}^\sharp, \sqsubseteq^{\mathbb{G}}, \sqcup^{\mathbb{G}}, \sqcap^{\mathbb{G}}, \perp^{\mathbb{G}}, \top^{\mathbb{G}})$$

$G \in \mathbb{G}^\sharp$: Representative of the Gaifman graph of Σ

Logic-based abstract domain

Abstract domain

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$$\mathcal{G}^\sharp = (\mathbb{G}^\sharp, \sqsubseteq^{\mathbb{G}}, \sqcup^{\mathbb{G}}, \sqcap^{\mathbb{G}}, \perp^{\mathbb{G}}, \top^{\mathbb{G}})$$

4. Shape-value domain (cofibered product of $\mathcal{G}^\sharp, \mathcal{N}^\sharp, \mathcal{D}^\sharp$)

$$\mathbb{M}^\sharp \triangleq \mathbb{G}^\sharp \Rightarrow (\mathbb{N}^\sharp \times \mathbb{W}^\sharp)$$

Logic-based abstract domain

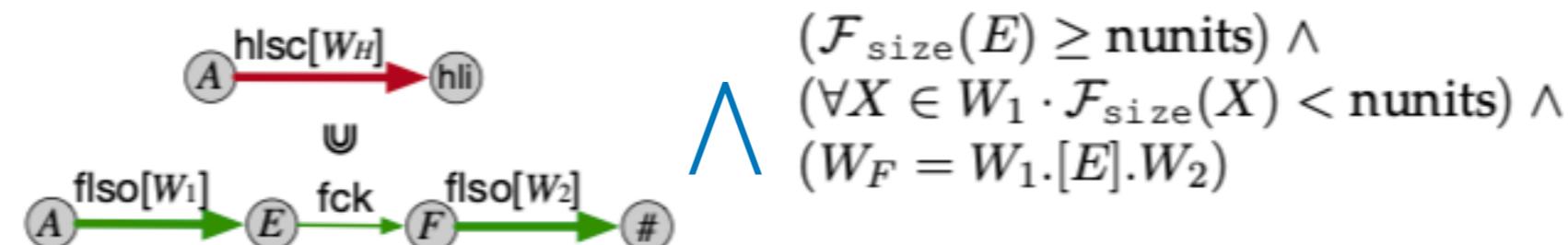
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Logic-based abstract domain

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$$\mathbb{M}^\# \triangleq \mathbb{G}^\# \Rightarrow (\mathbb{N}^\# \times \mathbb{W}^\#)$$

5. Disjunctive abstraction $\mathcal{A}^\#$

$$\mathbb{A}^\# \triangleq \mathcal{P}(\mathbb{M}^\#), \quad \gamma_{\mathbb{A}}(A^\#) \triangleq \bigcup \{\gamma_{\mathbb{M}}(m^\#) \mid m^\# \in A^\#\}$$

Logic-based abstract domain

Lattice operations: ordering and join

$$A^\# = (G, \Pi_N, \Pi_W) \in \mathbb{M}^\#, \quad B^\# = (G', \Pi'_N, \Pi'_W) \in \mathbb{M}^\#$$

$$A^\# \sqsubseteq^{\mathbb{M}} B^\# \quad \text{i.e. } G \sim_\sigma G' \quad \wedge \quad (\Pi_N \sqsubseteq^{\mathbb{N}} \Pi'_N \wedge \Pi_W \sqsubseteq^{\mathbb{W}} \Pi'_W)$$

$$A^\# \sqcup^{\mathbb{M}} B^\# \quad \text{i.e. } G_\sigma \wedge (\Pi_N \sqcup^{\mathbb{N}} \Pi'_N) \wedge (\Pi_W \sqcup^{\mathbb{W}} \Pi'_W)$$

Logic-based abstract domain

Lattice operations: ordering and join

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$$A^\# \sqcup^{\mathbb{M}} B^\# \quad \text{i.e. } G_\sigma \wedge (\Pi_N \sqcup^{\mathbb{N}} \Pi'_N) \wedge (\Pi_W \sqcup^{\mathbb{W}} \Pi'_W)$$

Theorem: soundness of $\sqsubseteq^{\mathbb{M}}$, $\sqcup^{\mathbb{M}}$

If $A^\# \sqsubseteq^{\mathbb{M}} B^\#$, then $\gamma_{\mathbb{M}}(A^\#) \subseteq \gamma_{\mathbb{M}}(B^\#)$

For any $A^\#, B^\# \in \mathbb{M}^\#$, $\gamma_{\mathbb{M}}(A^\#) \cup \gamma_{\mathbb{M}}(B^\#) \subseteq \gamma_{\mathbb{M}}(A^\# \sqcup^{\mathbb{M}} B^\#)$

Logic-based abstract domain

Lattice operations **folding**: eliminate nodes not labeled by program variables by applying lemmas:

- Predicate definition $P(\dots) \triangleq \vee_i \phi_i$ gives

$$\phi_i \Rightarrow P(\dots)$$

- List segment composition $P \in \{\mathbf{hls}, \mathbf{hlsc}, \mathbf{fls}, \mathbf{flso}\}$:

$$P(X; Y)[W_1] \star P(Y; Z)[W_2] \wedge W = W_1 . W_2 \Rightarrow P(X; Z)[W]$$

- blk lemmas, e.g. :

$$\mathbf{blk}(X; Y) \star \mathbf{blk}(Y; Z) \wedge X \leq Y \leq Z \Rightarrow \mathbf{blk}(X; Z)$$

Logic-based abstract domain

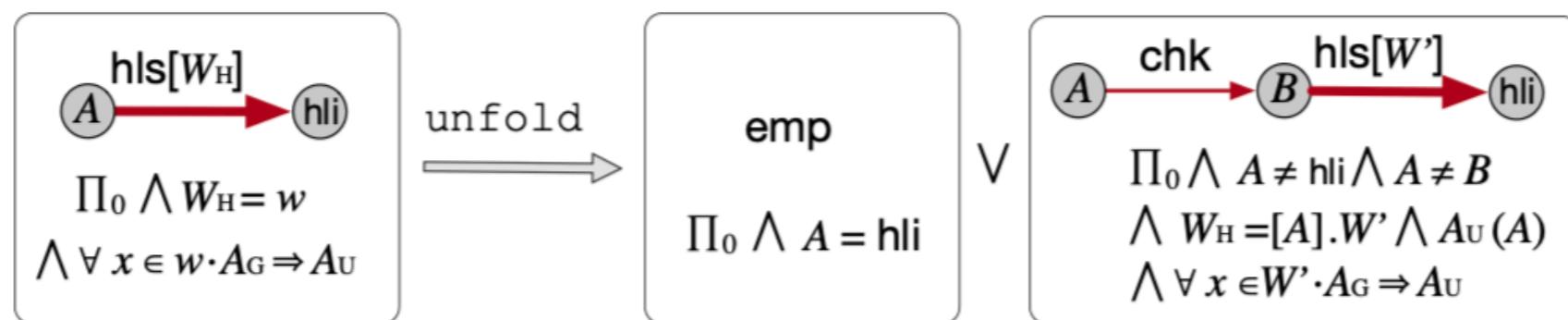
Lattice operation materialisation: unfolding summary

$$\mathbf{Unfold}^\sharp : A^\sharp \rightarrow \mathcal{P}_{fin}(A^\sharp) \quad (A^\sharp \in \mathbb{M}^\sharp)$$

Logic-based abstract domain

Lattice operation materialisation: unfolding summary

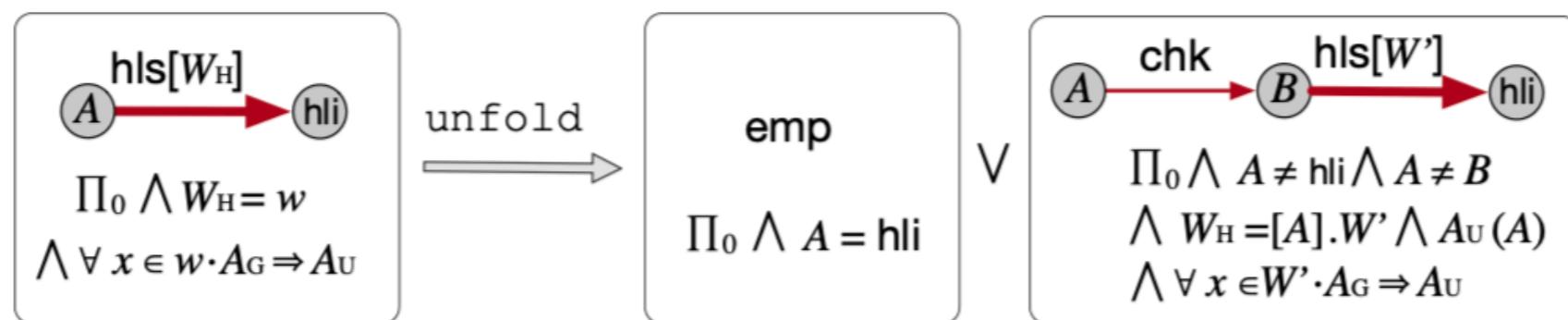
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Logic-based abstract domain

Lattice operation materialisation: unfolding summary

$$\mathbf{Unfold}^\sharp : A^\sharp \rightarrow \mathcal{P}_{fin}(A^\sharp) \quad (A^\sharp \in \mathbb{M}^\sharp)$$



Theorem: soundness of \mathbf{Unfold}^\sharp

If \mathbf{Unfold}^\sharp transforms A^\sharp into a finite number of disjunctions

$$A_1^\sharp \vee A_2^\sharp \vee \dots \vee A_n^\sharp, \text{ then } \gamma_{\mathbb{M}} \subseteq \bigcup_{0 \leq i \leq n} \gamma_{\mathbb{M}}(A_i^\sharp)$$

Fields and Hierarchical Unfolding

Let fix $\mathbf{blk} \prec_P \mathbf{chd} \prec_P \mathbf{chk} \prec_P \mathbf{fck} \prec_P \mathbf{hls}, \mathbf{hlsc}, \mathbf{fls}, \mathbf{flso}$ ($Q \leq_P P \triangleq (Q \prec_P P) \vee (Q = P)$)

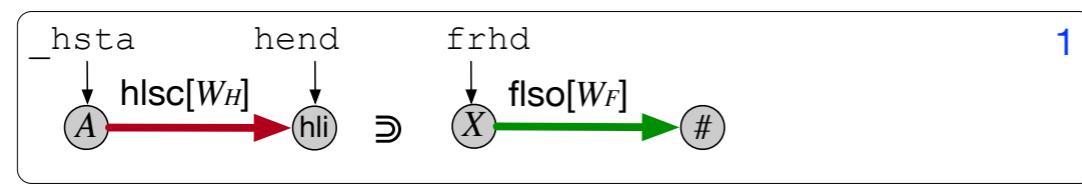
Given an atom $P(X; \dots)$ and a statement s accessing X ,

then **apply rules of (unfold)** P to obtain atom $Q(X; \dots)$ s.t. $Q \leq_P P$ and:

- if s reads $X.f$, then $Q \leq_P \mathbf{fck}$,
- if s assigns $X.isfree$ or $X.fnx$, then $Q \leq_P \mathbf{chk}$,
- if s mutates X using pointer arithmetic or assigns $X.size$, then $Q \leq_P \mathbf{chd}$.

Logic-based abstract domain

Hierarchical folding and unfolding



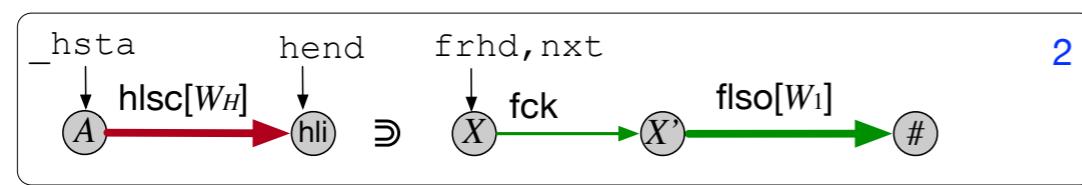
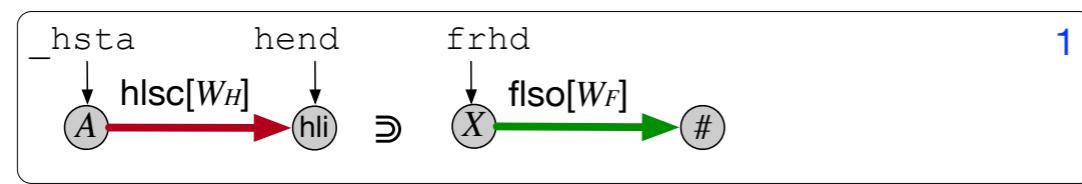
1

```
void* malloc(size_t nbytes) {  
    HDR *nxt, *prv;  
    size_t nunits =  
        (nbytes+sizeof(HDR)-1)/sizeof(HDR) + 1;  
    for (prv = NULL, nxt = frhd; nxt;  
         prv = nxt, nxt = nxt->fnx) {  
        if (nxt->size >= nunits) {  
            if (nxt->size > nunits) {  
                nxt->size -= nunits;  
                nxt += nxt->size;  
                nxt->size = nunits;  
            } else {  
                if (prv == NULL)  
                    frhd = nxt->fnx;  
                else  
                    ...  
        }  
    }  
}
```

before loop

Logic-based abstract domain

Hierarchical folding and unfolding

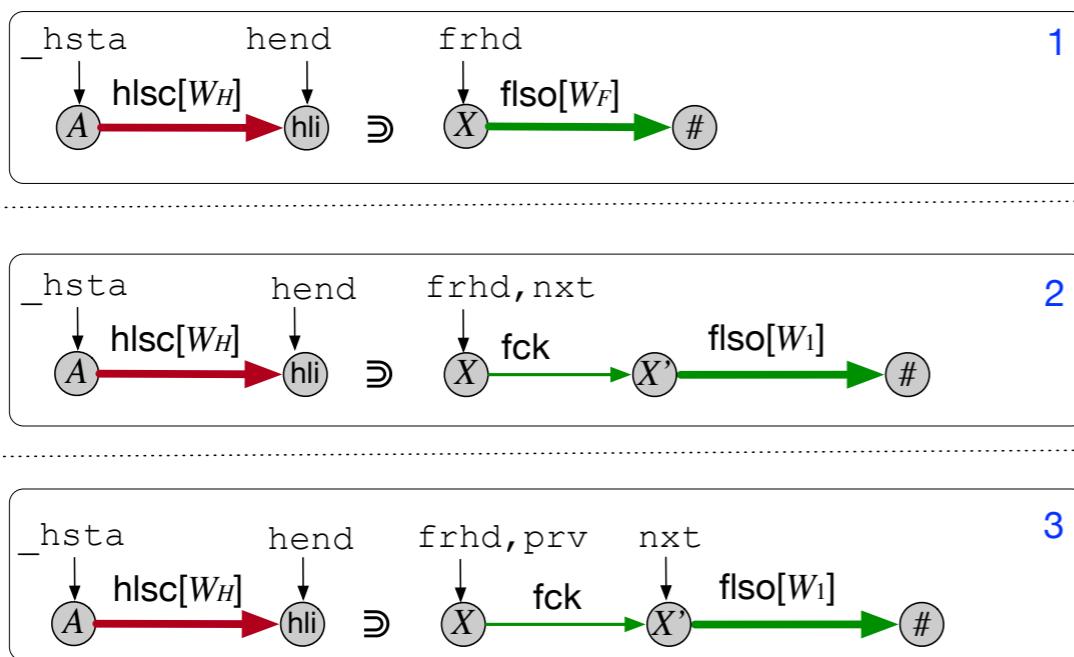


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void* malloc(size_t nbytes) {  
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    size_t nunits =  
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    for (prv = NULL, nxt = frhd; nxt;  
         prv = nxt, nxt = nxt->fnx) {  
        if (nxt->size >= nunits) {  
            if (nxt->size > nunits) {  
                nxt->size -= nunits;  
                nxt += nxt->size;  
                nxt->size = nunits;  
            } else {  
                if (prv == NULL)  
                    frhd = nxt->fnx;  
                else  
                    ...  
        }  
    }  
}
```

Unfold free list summary

Logic-based abstract domain

Hierarchical folding and unfolding

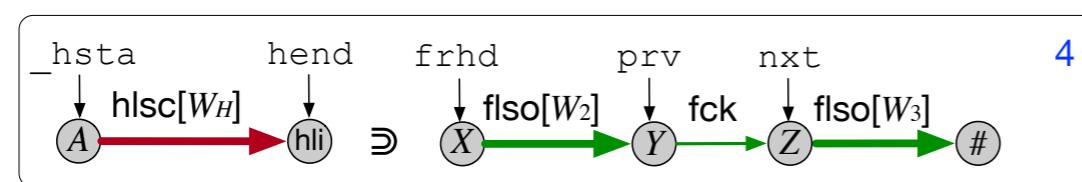
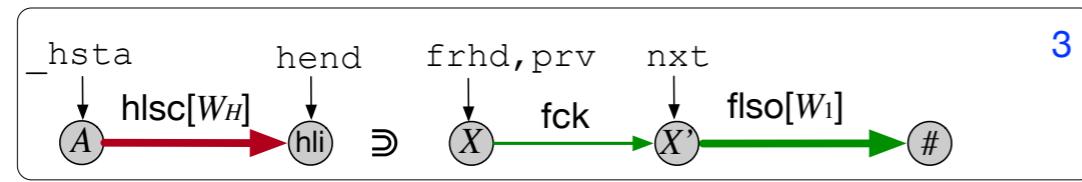
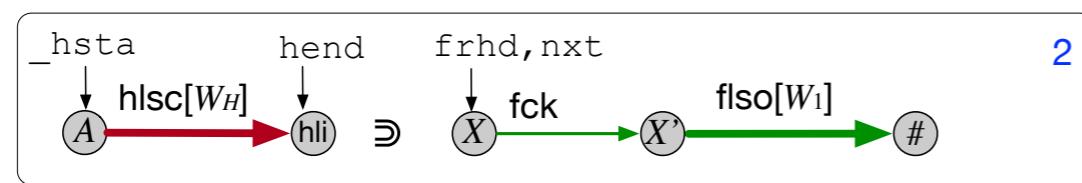
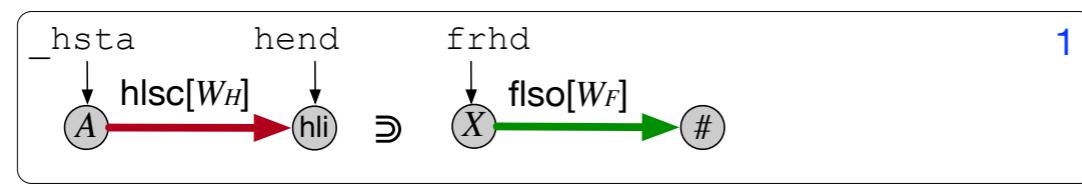


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    size_t nunits =  
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    for (prv = NULL, nxt = frhd; nxt;  
         prv = nxt, nxt = nxt->fnx) {  
        if (nxt->size >= nunits) {  
            if (nxt->size > nunits) {  
                nxt->size -= nunits;  
                nxt += nxt->size;  
                nxt->size = nunits;  
            } else {  
                if (prv == NULL)  
                    frhd = nxt->fnx;  
                else  
                    ...  
        }  
    }  
}
```

Unfold free list summary

Logic-based abstract domain

Hierarchical folding and unfolding

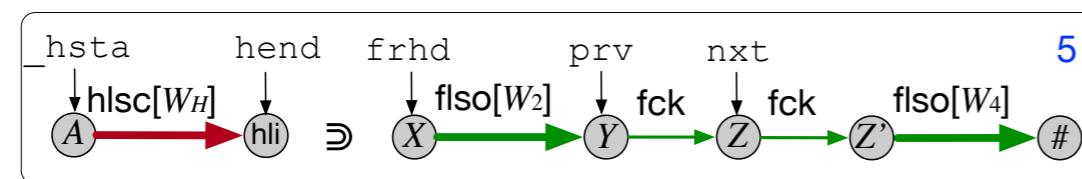
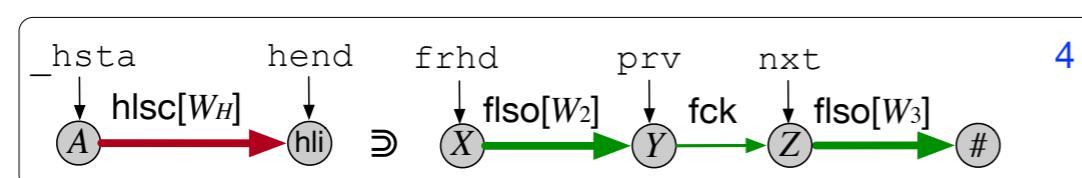
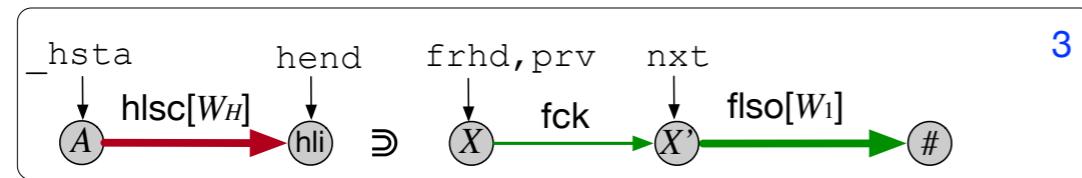
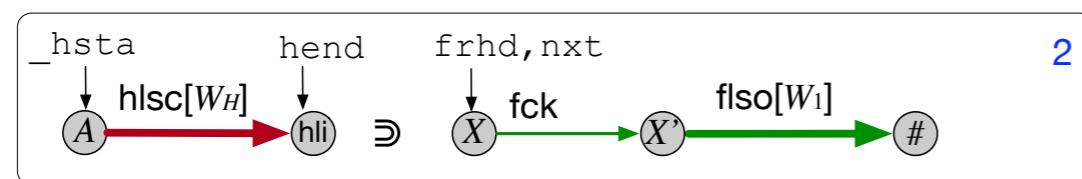
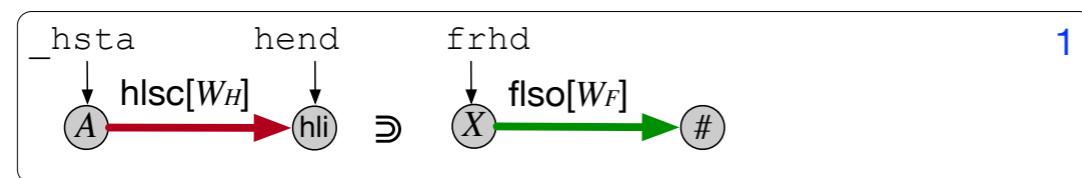


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    size_t nunits =  
        (nbytes+sizeof(HDR)-1)/sizeof(HDR) + 1;  
    for (prv = NULL, nxt = frhd; nxt;  
         prv = nxt, nxt = nxt->fnx) {  
        if (nxt->size >= nunits) {  
            if (nxt->size > nunits) {  
                nxt->size -= nunits;  
                nxt += nxt->size;  
                nxt->size = nunits;  
            } else {  
                if (prv == NULL)  
                    frhd = nxt->fnx;  
                else  
                    ...  
        }  
    }  
}
```

i-th iteration

Logic-based abstract domain

Hierarchical folding and unfolding

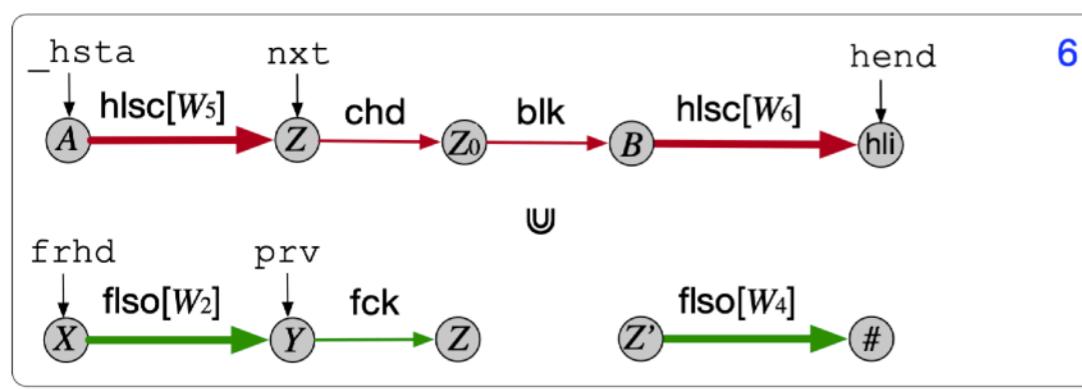
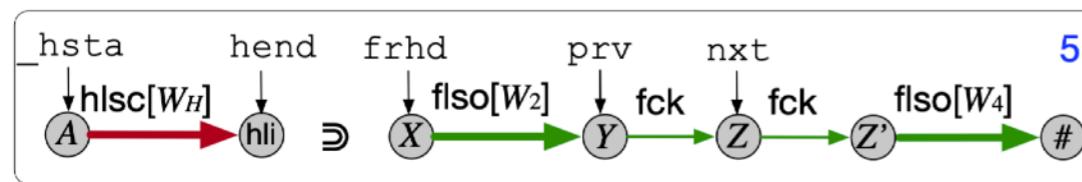


```
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    for (prv = NULL, nxt = frhd; nxt;  
         prv = nxt, nxt = nxt->fnx) {  
        if (nxt->size >= nunits) {  
            if (nxt->size > nunits) {  
                nxt->size -= nunits;  
                nxt += nxt->size;  
                nxt->size = nunits;  
            } else {  
                if (prv == NULL)  
                    frhd = nxt->fnx;  
                else  
                    ...  
            }  
        }  
    }  
}
```

read size field

Logic-based abstract domain

Hierarchical folding and unfolding

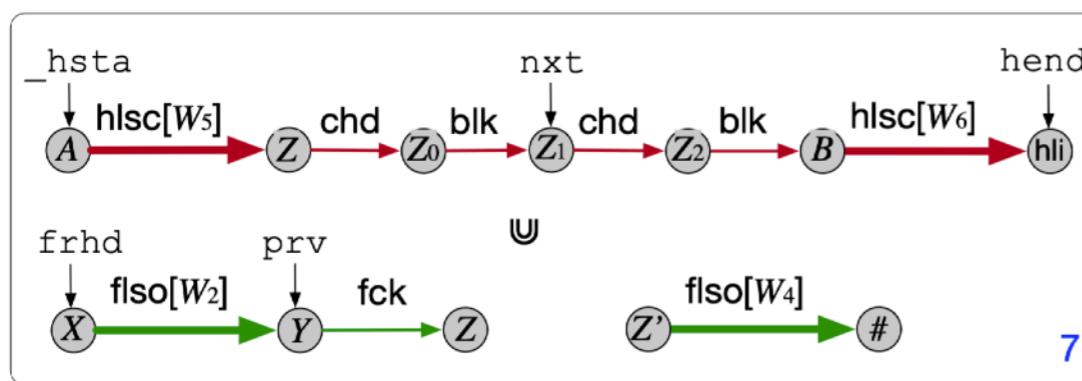
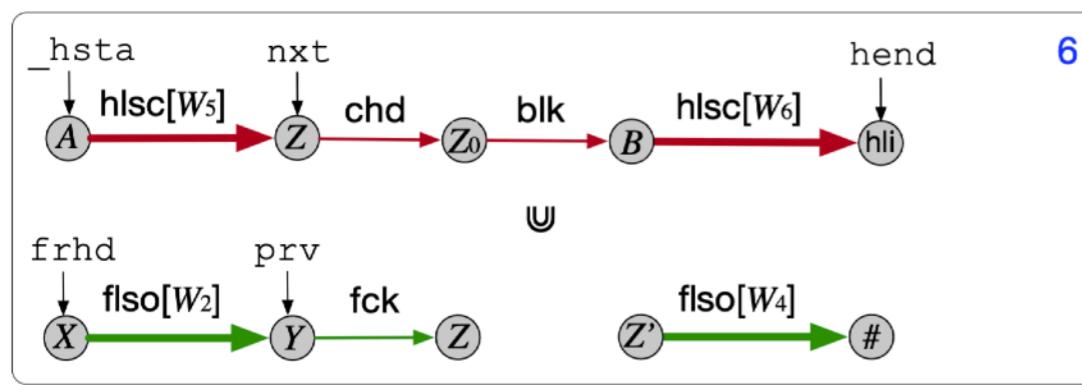
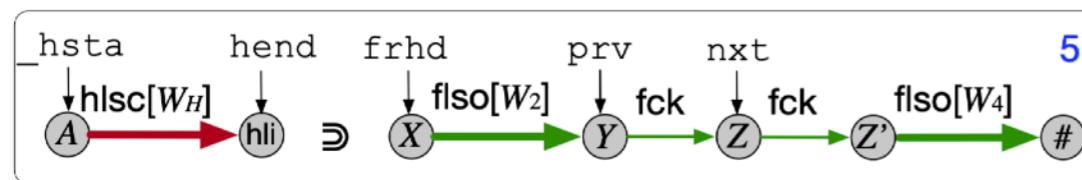


```
void* malloc(size_t nbytes) {  
    HDR *nxt, *prv;  
    size_t nunits =  
        (nbytes+sizeof(HDR)-1)/sizeof(HDR) + 1;  
    for (prv = NULL, nxt = frhd; nxt;  
         prv = nxt, nxt = nxt->fnx) {  
        if (nxt->size >= nunits) {  
            if (nxt->size > nunits) {  
                nxt->size -= nunits;  
                nxt += nxt->size;  
                nxt->size = nunits;  
            } else {  
                if (prv == NULL)  
                    frhd = nxt->fnx;  
                else  
                    ...  
            }  
        }  
    }  
}
```

write size field

Logic-based abstract domain

Hierarchical folding and unfolding



```

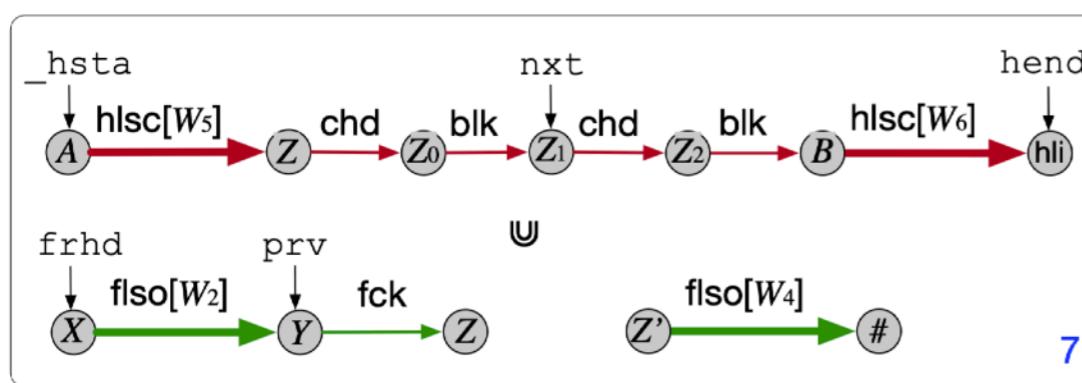
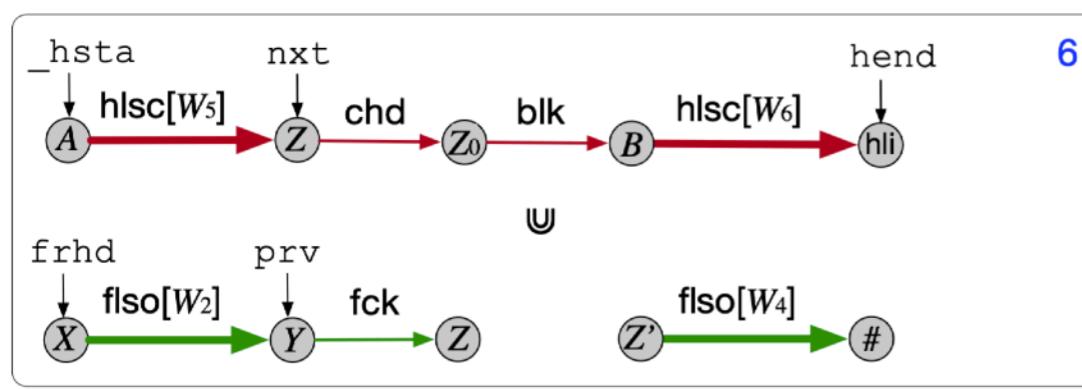
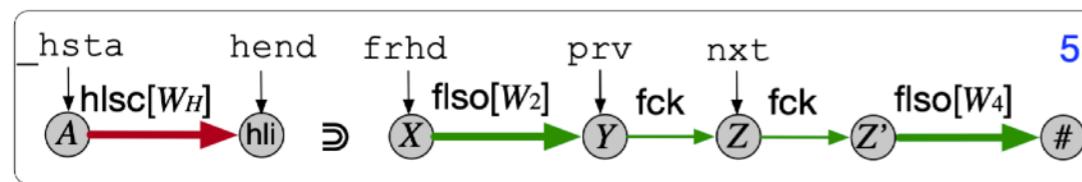
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...

write size field

Logic-based abstract domain

Hierarchical folding and unfolding



```

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                    frhd = nxt->fnx;
                else
                    ...

```

write size field

Experimental

Static analyser MMEN

- Frama-c plugin (Ocaml 38k LOC)
- Pointer arithmetics
- Low level system calls, e.g., sbrk
- Verifies a set of DMAs

LOPSTR'16

Future work

- Modelling and verification for **concurrent** memory algorithms (B, CIVL, etc)
- Other components of OS kernel
- Extension of the logic
- Scalable analysis tool

Publications

2018	<p>Tool paper: Static Analyser for Dynamic Memory Allocators (submit soon)</p> <p>Journal paper: Hierarchical Shape Abstraction for Analysis of Dynamic Memory Allocators</p>
2017	<p>Formal Modelling of List Based Dynamic Memory Allocators.</p> <p>Bin Fang, Mihaela Sighireanu, Geguang Pu. Journal of SCIENCE CHINA Information Sciences, 2017.</p>
2017	<p>A Refinement Hierarchy for Free List Memory Allocators.</p> <p>Bin Fang, Mihaela Sighireanu. ACM SIGPLAN International Symposium on Memory Management (ISMM) 2017.</p>
2016	<p>Hierarchical Shape Abstraction of Free–List Memory Allocators.</p> <p>Bin Fang, Mihaela Sighireanu. 26th International Symposium on Logic–Based Program Synthesis and Transformation LOPSTR 2016.</p>
2015	<p>Formal Development of a Real–Time Operating System Memory Manager.</p> <p>Wen Su, Jean–Raymond Abrial, Geguang Pu, Bin Fang. 20th International Conference on Engineering of Complex Computer Systems ICECCS 2015.</p>
2014	<p>Automated Coverage–Driven Test Data Generation Using Dynamic Symbolic Execution.</p> <p>Ting Su, Siyuan Jiang, Geguang Pu, Bin Fang, Jifeng He, Jun Yan, Jianjun Zhao. Eighth International Conference on Software Security and Reliability, SERE 2014.</p>
2014	<p>Runtime Verification by Convergent Formula Progression.</p> <p>Yan Shen, Jianwen Li, Zheng Wang, Bin Fang, Geguang Pu and Wangwei Liu. 21st Asia–Pacific Software Engineering Conference APSEC 2014.</p>

Thank you! Questions ?